Tektronix®

DDR3 and LPDDR3 Measurement and Analysis

6 Series MSO Opt. 6-CMDDR3 and Opt. 6-DBDDR3 Application Datasheet

DDR3/LPDDR3 Measurement and Analysis for memory designs

Get more visibility into your memory designs with the Tektronix DDR3/LPDDR3 Automated Conformance package (Opt. 6-CMDDR3) and DDR3/LPDDR3 Measurement and Analysis function (Opt. 6-DBDDR3) on the 6 Series MSO. The integration of the DDR software, oscilloscope, high-performance analog and digital probes lets you perform detailed, accurate amplitude, timing, and eye diagram measurements on your DDR designs to verify compliance with the Joint Electronic Device Engineering Council (JEDEC) electrical and timing specifications. The digital probes help get insight on the control signals of the DDR bus. The 12-bit analog-to-digital converters in the 6 Series MSO deliver high-precision measurement data with the lowest noise in the industry to let you achieve new levels of debugging efficiency and measurement reliability.

Key features

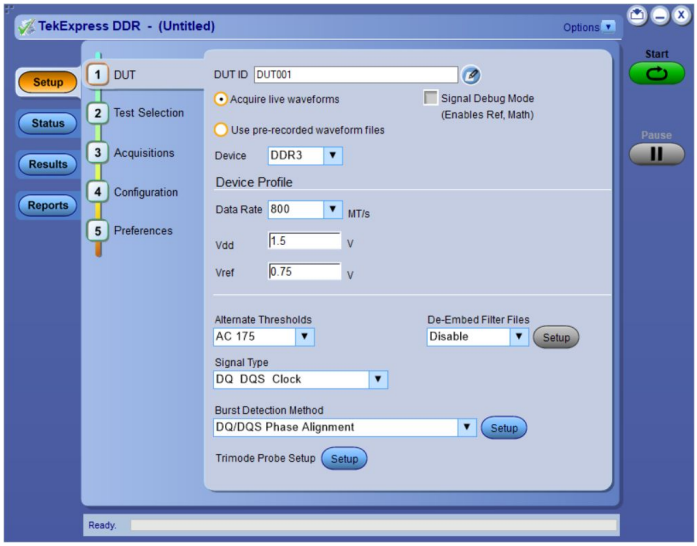
- Complete test coverage and fully automated conformance testing of DDR3 and LPDDR3 measurements as per the specification, including Eye diagram test on data and clock.
- Ability to simultaneously define Read and Write searches and perform specific DDR measurements on the qualified bursts over long record lengths.
- Ability to set voltage threshold levels per measurement as per the specification.
- Intuitive user interface and workflow to configure and perform DDR electrical validation.
- Easily switch from Conformance test environment to Debug environment on the scope to get deeper insights into test failures.
- Optionally save setup files in Conformance test suite, to be able to recall the scope state post execution.
- Automated report generation saves measurements, test results, and waveform images in .MHT, .CSV or .PDF file format. CSV format helps to parse and customize the test reports as per users' needs

  Supports a wide range of interposers for different memory standards, along with best-in-class probes, to meet signal integrity requirements.

DDR3/LPDDR3 automated testing with Opt 6-CMDDR3

Opt. 6-CMDDR3 solution lets you perform automated DDR3 and LPDDR3 conformance testing. This solution works in conjunction with Opt. 6-DBDDR3 to add specific measurements, configure these measurements and fetch the results post analysis. This helps the user to avoid manually save and recall scope setup files. The python sequencer enables fast execution of 100+ measurements, ensures test validation in completed quickly.

The DUT panel lets you choose the device type and device profile which includes the speed grade supported by the DDR device and configure the Vdd and Vref settings.



6-CMDDR3 DUT panel

The user can choose to optionally provide the filter files (.flt) relative to the hardware components used in the signal path, which will be de-embedded from the captured signal prior to analysis using the scope MATH subsystem.

DDR signal is bursty in nature and one of the first steps when it comes to DDR testing is to separate and qualify valid Read and Write bursts. The measurements are then performed on these qualified bursts.

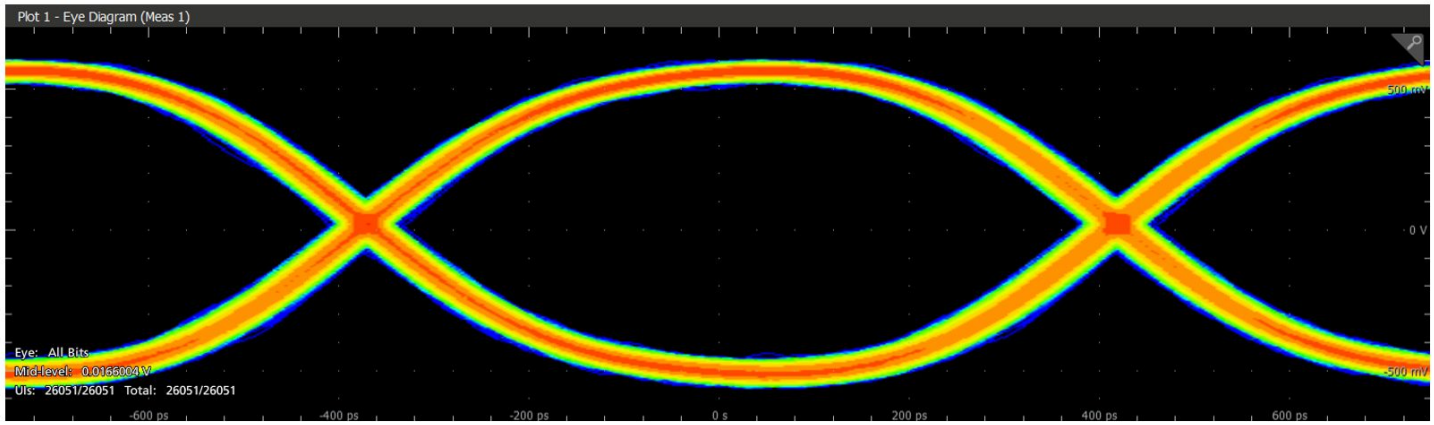
The DUT panel provides user with a choice of several burst detection methods:

Depending on the probing mechanism, user can choose the signal type settings which helps configure the signal sources accordingly during execution.

By using probe mode, user can change the probe configurations.

Opt. 6-CMDDR3 supports the 'Signal Debug' mode in the DUT panel. This mode helps the user to configure the scope settings manually without the settings being overridden by the automation software. In this mode, user can provide Channels, References or MATHs as inputs to the software.

The test selection panel lists the DDR measurements as logical groups depending on the signal type selection in the DUT panel. This helps user to complete the automated measurements with no manual intervention. Eye diagram tests on Data and Clock signals are enabled beyond the conformance requirement, so user gets deeper insight into the memory designs.



6-CMDDR3 running a DDR3 Clock Eye diagram

Once the execution is completed, the software generates a detailed test report with setup information, test summary and detailed results with pass fail status, limits and test specific images.

Tektronix

TekExpress DDR Report

Report for DDR3 Measurements

Setup Information			
DUT ID	DUT001	TekExpress DDR	1.0.0.61
Date/Time	2019-04-02 00:59:15	TekExpress FrameWork Version	4.9.999.28_INTERNAL
Suite	Transmitter	TekScope Model	MSO64
Acquisition Mode	Live	TekScope Firmware	1.14.3.5997
Vdd	1.5 V	Probe CH1 Model	TDP7708
Vref	0.75 V	Probe CH1 Serial number	Q100025
Alternate Threshold	AC 175	Probe CH2 Model	TDP7708
Data Rate	800 MT/s	Probe CH2 Serial number	Q100008
Over All Test Result	Pass	Probe CH3 Model	TDP7708
Total Execution Time	58 Seconds	Probe CH3 Serial number	P100003
		Probe CH4 Model	TLP058
		Probe CH4 Serial number	PQ10011
DUT COMMENT:	General Comment – DDR3		

Data Eye Height	Pass
Data Eye Width	Pass

Data Eye Height

Measurement Group	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Additional Information
Read Burst	Data Eye Height	918.447	mV	Informative	N.A	N.A	N.A	Min = 812.509 mV, Max = 1.328 V, Search Events = 150.
COMMENTS	N.A							

Back to Summary Table

Data Eye Width

Measurement Group	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Additional Information
Read Burst	Data Eye Width	1.175	ns	Informative	N.A	N.A	N.A	Min = 1.128 ns, Max = 1.298 ns, Search Events = 150.
COMMENTS	N.A							

Back to Summary Table

Data Eye Height

DDR3_800_Read_Burst_Eye_Diagram

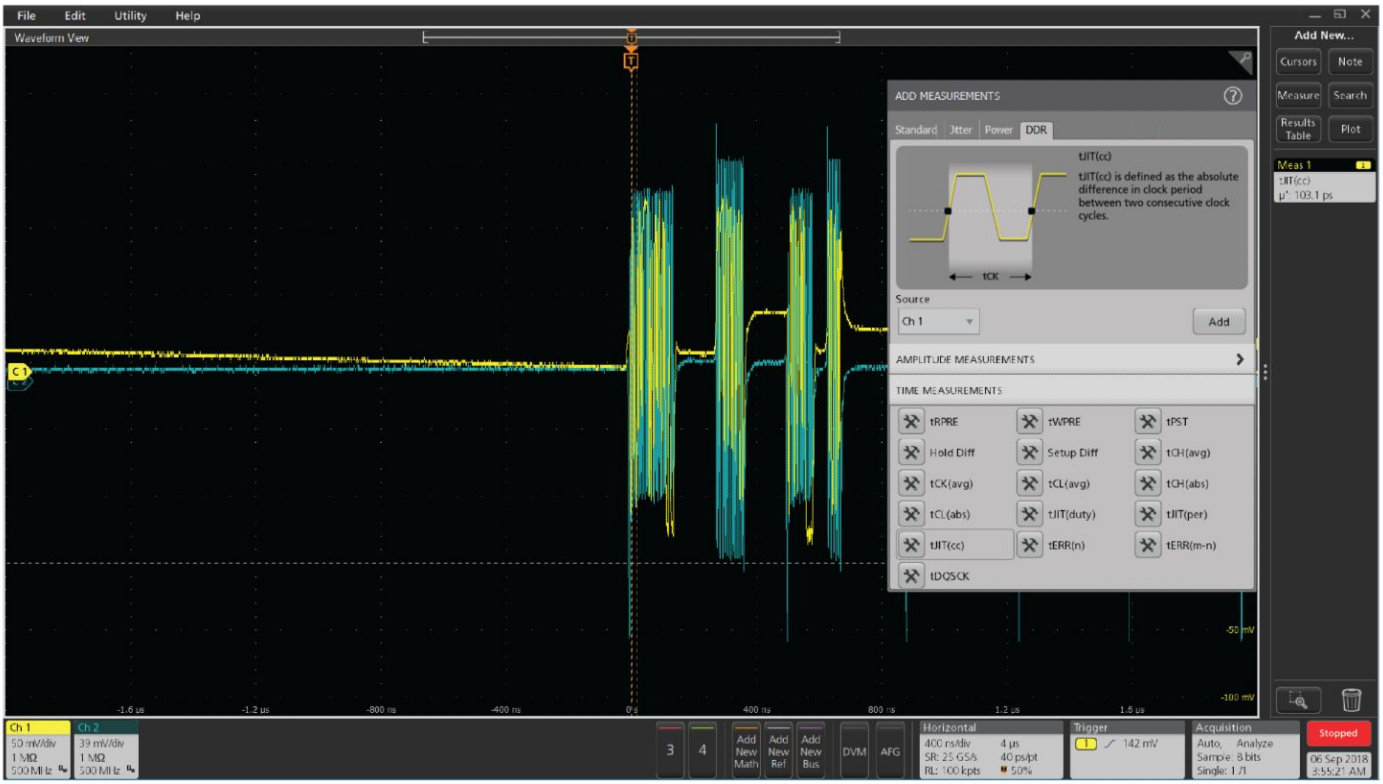
6-CMDDR3 Report file with DDR3 Eye diagram test result

To debug test failures, Tektronix offers 6-DBDDR3 measurement package integrated into the scope measurement subsystem, which helps the user to easily configure and test their memory designs.

DDR3 debug with Opt 6-DBDDR3

Opt.6-DBDDR3 lets you capture long records, automatically separate Read and Write bursts based on selected measurements, and perform measurements over multiple Read or Write bursts. You can define multiple Read and Write searches and continuously run the DDR3/LPDDR3 measurements on the qualified searches and perform statistical analysis on the results.

DDR3 electrical testing and timing analysis requires a 6 Series MSO oscilloscope with a recommended bandwidth of 8 GHz to cover entire range of DDR3 speed grades. However, for signal integrity testing and debug, a minimum bandwidth of 4 GHz would suffice most of the user's needs.



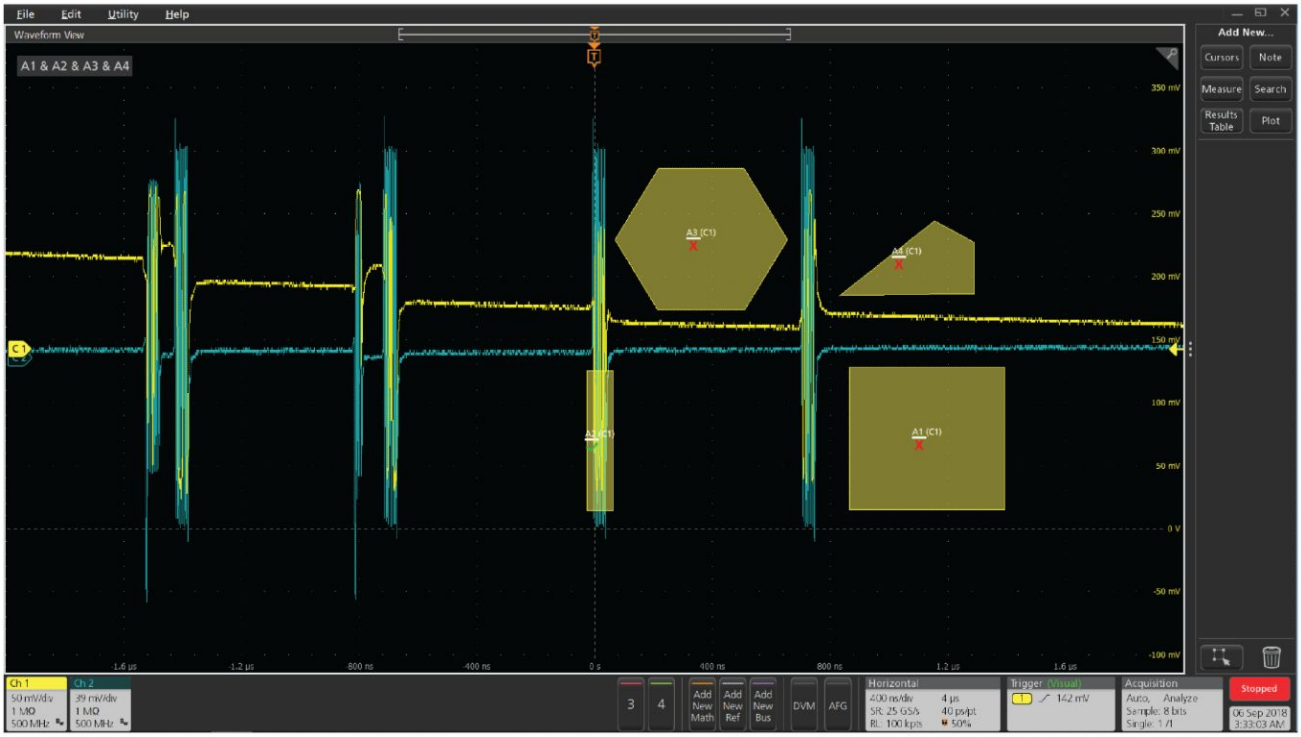
Just two screen taps are needed to open the DDR measurement menu.

Automated read and write burst detection

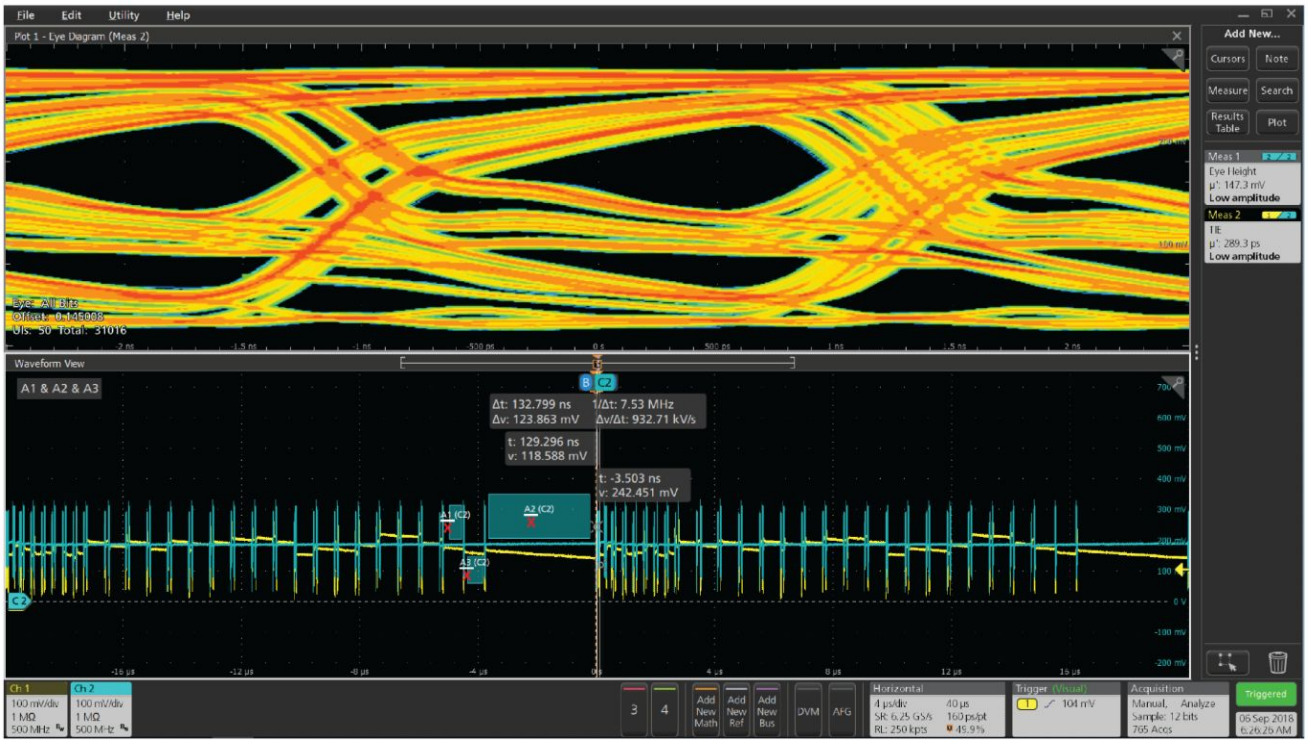
Some JEDEC conformance measurements require isolating the events of interest such as read or write bursts on the memory bus, which is automatically handed by the Conformance solution.

For debug, it may be necessary to further isolate certain events by a particular rank or bank, or to isolate certain data patterns for analysis of signal-integrity issues such as data-dependent jitter, timing, or noise problems. The simplest way to achieve this is to use the DQS (Data Strobe signal) to identify the start of a read or write burst. For example, DDR3 always asserts DQS high at the start of a write, or low at the start of a read.

The Visual Trigger feature on the 6 Series MSO oscilloscope lets you further condition traditional triggers for more versatile DQS burst capture capability. Visual Trigger lets you create mask-like areas directly on the waveform display, where the boundaries of the areas help define trigger events for a DQS or Data Strobe signal.



Visual Trigger lets you add standard or user-specified areas to trigger the DDR3 waveform on specific trigger conditions.



An Eye diagram of a DDR3 signal using Opt. 6-DJA measurement and Visual Trigger conditioning on the source waveform.

Making the complex easier

The JEDEC specifications for each memory technology specifies an array of conformance measurements. These measurements include clock jitter, setup and hold timing, transition voltages, signal overshoot and undershoot, slew rate and other electrical-quality tests. These tests are complex to measure using general-purpose tools.

Because the JEDEC-specified measurement methods require reference levels, pass/fail limits, and more, it is extremely valuable to have an application-specific measurement utility for DDR testing. Opt. 6-CMDDR3 is designed to correctly set up DDR measurements for specified devices. The broad set of measurements available in 6-CMDDR3 conforms to the JEDEC specifications. You can also leverage Opt. 6-DBDDR3 to customize settings to measure non-standard devices or system implementations.

Option 6-CMDDR3 works with option 6-DJA (Advanced Jitter Analysis) to provide Jitter and Eye Diagram Analysis Tools. These two utilities work together to create a powerful, flexible, and easy-to-use test suite for DDR testing and debug.

DDR search feature

The DDR search feature lets you search an entire waveform acquisition for specific signal conditions, such as DDR Read/Write, and mark the waveform where the conditions are met. In addition to using these marks for visual analysis, the oscilloscope can apply the marks as qualifiers for DDR-specific measurements, so that the measurements occur only on the appropriate portion of the data stream. The search algorithms in DDR search make use of the fact that DDR phase relationships are different for read and write bursts; DQ and DQS are in-phase for reads, and 90 degrees out-of-phase for writes. It also supports burst identification based on Chip Select (CS) signal and digital signals (Chip Select-CS, Row Access Strobe-RAS, Column Access Strobe-CAS, and Write Enable source-WE).

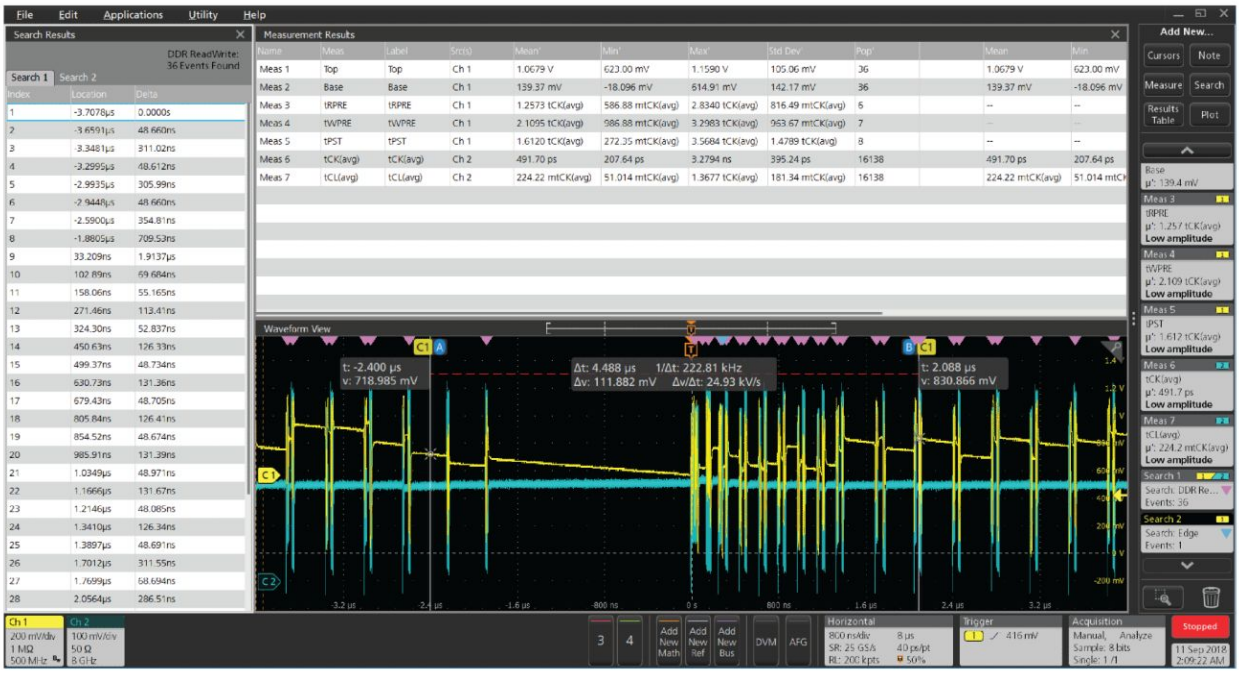
Steps to debug failures

The first step in memory debugging is to define a search. This can be done by clicking on the Search button on the scope and defining a DDR search on Read or Write bursts. The next step is to add the measurement from DDR tab and configure these measurements. The configuration involves providing search as an input to the measurement and defining signal sources. Since there are multitude of measurements to be configured, it is recommended to configure the measurements manually one time and save the scope setup file. When you want to debug next time, it is easy to recall the scope setup file, which brings back all the configured measurements on the scope and make edits as necessary.

Once the setup is complete and you select <Run> (or <Single>), the oscilloscope acquires the signals of interest, identifies and marks qualified data bursts, and updates the results for the selected measurements.

The factory setup files supplied with 6-DBDDR3 package are built with industry-standard measurement settings, you may need to modify the settings one time and save them if your test setup is different than the default setup files.

You can view results in table format by clicking on Results Table button on the scope screen. The results table displays all measurement results with their statistical population, sources and other relevant data. You can generate a report, with an option to save the waveform data that is used to make these measurements.



Detailed results showing qualified bursts of a DDR3 signal.

Measurement Report Tektronix

Tuesday September 11 2018 02:27:11

Setup Configuration

Scope Details			
Scope Model Number	Scope Serial Number	TekScope Version	Scope Calibration Status
MSO64	QU100005	1.11.30	Fail

Measurement Result Details

Name	Meas	Sources	Mean'	Min'	Max'	Pk-Pk'	Std Dev'	Pop'	Accum Mean	Accum Min	Accum Max	Accum Pk-Pk	Accum Std Dev	Accum Pop
Meas1	Data Eye Height	Ref1 Ref2	572.0 mV	459.1 mV	649.4 mV	190.3 mV	40.29 mV	24	572.0 mV	459.1 mV	649.4 mV	190.3 mV	40.29 mV	24
Meas2	Data Eye Width	Ref1 Ref2	981.9 ps	819.2 ps	1.060 ns	240.4 ps	51.64 ps	24	981.9 ps	819.2 ps	1.060 ns	240.4 ps	51.64 ps	24
Meas3	VOH(AC) DQ	Ref1	1.181 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95	1.181 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95
Meas4	VOH(DC) DQ	Ref1	1.181 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95	1.181 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95
Meas5	VOL(AC)DQ	Ref1	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95
Meas6	VOL(DC) DQ	Ref1	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95
Meas7	tDIPW-High	Ref1	2.308 ns	587.5 ps	10.14 ns	9.551 ns	1.785 ns	95	2.308 ns	587.5 ps	10.14 ns	9.551 ns	1.785 ns	95
Meas8	tDIPW-Low	Ref1	2.291 ns	244.5 ps	9.929 ns	9.685 ns	1.726 ns	108	2.291 ns	244.5 ps	9.929 ns	9.685 ns	1.726 ns	108
Meas9	SRQse-Fall(DQ)	Ref1	-5.674 V/ns	-9.972 V/ns	-878.0 mV/ns	9.094 V/ns	1.736 V/ns	98	-5.674 V/ns	-9.972 V/ns	-878.0 mV/ns	9.094 V/ns	1.736 V/ns	98
Meas10	SRQse-Rise(DQ)	Ref1	3.483 V/ns	1.059 V/ns	5.052 V/ns	3.993 V/ns	661.1 mV/ns	106	3.483 V/ns	1.059 V/ns	5.052 V/ns	3.993 V/ns	661.1 mV/ns	106
Meas11	VOHdiff(AC)	Ref2	910.7 mV	726.0 mV	990.0 mV	264.0 mV	60.66 mV	220	910.7 mV	726.0 mV	990.0 mV	264.0 mV	60.66 mV	220
Meas12	VOLdiff(AC)	Ref2	-845.9 mV	-942.0 mV	-762.0 mV	180.0 mV	36.86 mV	220	-845.9 mV	-942.0 mV	-762.0 mV	180.0 mV	36.86 mV	220
Meas13	tDQSCK-Diff	Ref3 Ref2	106.3 ps	-1.237 ns	1.227 ns	2.463 ns	712.1 ps	219	106.3 ps	-1.237 ns	1.227 ns	2.463 ns	712.1 ps	219
Meas14	tDQSQ-Diff	Ref1 Ref2	33.10 ps	-452.8 ps	189.2 ps	642.0 ps	119.7 ps	218	33.10 ps	-452.8 ps	189.2 ps	642.0 ps	119.7 ps	218
Meas15	tDVAC(DQS)	Ref2	1.100 ns	0.000 s	1.287 ns	1.287 ns	262.3 ps	464	1.100 ns	0.000 s	1.287 ns	1.287 ns	262.3 ps	464
Meas16	tQH	Ref2 Ref1	1.303 ns	629.5 ps	1.478 ns	848.9 ps	108.0 ps	205	1.303 ns	629.5 ps	1.478 ns	848.9 ps	108.0 ps	205
Meas17	tQSH	Ref2	1.167 ns	301.8 ps	1.351 ns	1.049 ns	268.5 ps	244	1.167 ns	301.8 ps	1.351 ns	1.049 ns	268.5 ps	244
Meas18	tQSL	Ref2	1.238 ns	1.184 ns	1.319 ns	134.9 ps	26.68 ps	220	1.238 ns	1.184 ns	1.319 ns	134.9 ps	26.68 ps	220
Meas19	tRPRE	Ref2	1.065 tCK(avg)	1.045 tCK(avg)	1.087 tCK(avg)	51.32 mtCK(avg)	11.04 mtCK(avg)	24	1.065 tCK(avg)	1.045 tCK(avg)	1.087 tCK(avg)	51.32 mtCK(avg)	11.04 mtCK(avg)	24
Meas20	tRPST	Ref2	286.9 mtCK(avg)	151.3 mtCK(avg)	447.0 mtCK(avg)	295.7 mtCK(avg)	131.6 mtCK(avg)	24	286.9 mtCK(avg)	151.3 mtCK(avg)	447.0 mtCK(avg)	295.7 mtCK(avg)	131.6 mtCK(avg)	24
Meas21	SRQdiff-Fall(DQS)	Ref2	-9.570 V/ns	-11.10 V/ns	-960.0 mV/ns	10.14 V/ns	750.4 mV/ns	221	-9.570 V/ns	-11.10 V/ns	-960.0 mV/ns	10.14 V/ns	750.4 mV/ns	221
Meas22	SRQdiff-Rise(DQS)	Ref2	7.746 V/ns	2.424 V/ns	9.208 V/ns	6.784 V/ns	1.398 V/ns	221	7.746 V/ns	2.424 V/ns	9.208 V/ns	6.784 V/ns	1.398 V/ns	221

Views

Time Domain View

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A detailed test report with setup details, measurement results and waveform image.

DDR3 main memory interposers

Gaining access to signal test points on a memory chip is a significant challenge in DDR testing. The JEDEC standards requires that measurements should be taken at the Ball Grid Array (BGA) ballouts of the memory component, connections that are very difficult to access.

Tektronix, in partnership with Nexus Technology [1], offers probing options such as BGA interposers that supports different memory devices in a variety of form factors. The interposer includes an embedded tip resistor placed close to the BGA pad. The DDR3 main memory is available in standard BGA component packages as well as dual-inline-memory-modules of DIMM and SODIMM.

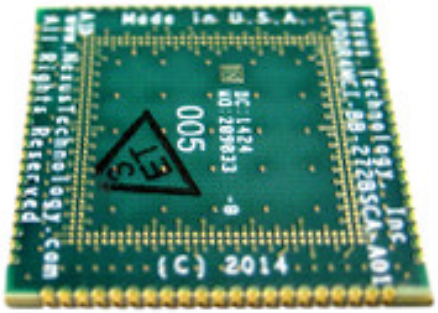
Standard BGA packages are soldered directly to the printed circuit board (PCB) while modules comprise a series of packages in a standard PCB format with standard connections between the DIMM and the main board. Interposers are available for both component packages and DIMM and SODIMM modules.

Introduction of an interposer and an oscilloscope probe may change the characteristics of the signal. Apply de-embedding filters to remove the effect of the interposer and a probe in the signal path to get an accurate representation of the signal at the probe point.

EdgeProbe Interposer

The Nexus Technology's patented EdgeProbe™ interposer is available for DDR3, LPDDR3, and other new memory products. It has a small mechanical footprint as the probe points are on the edge of the interposer. The probes can attach directly to the target device to provide access to the clock, command bus, data, strobe, and address signals.

The EdgeProbe design removes mechanical clearance issues as the interposers are the size of the memory components. Embedded resistors within the interposers place the oscilloscope probe tip resistor extremely close to the BGA pad, by providing an integrated oscilloscope probe on all the signals.



EdgeProbe interposer

Socketed Interposer

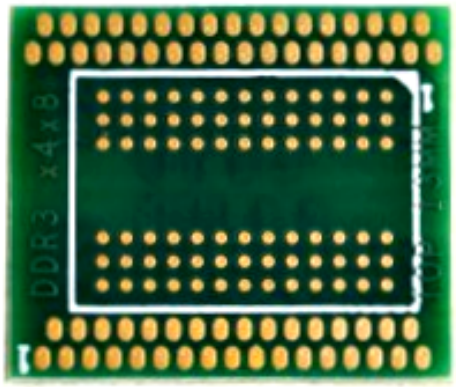
A socketed interposer typically provides access to all component signals and elevates the interposer above adjacent components for mechanical clearance. This solution offers a custom socket that is installed on the target and has an interposer that is installed by pressing it into the socket. Retention is designed into the solution since the interposer can be removed by pulling an unsecured interposer from the target socket.

The interposer can have the memory component soldered directly to it or optionally have a socket on the interposer. The socket on the interposer allows for memory components to be manually inserted and removed to easily evaluate different vendor memory components. When testing is completed, the interposer can be removed and the memory device inserted directly into the custom socket on the target, removing the effect of the interposer.

1 For a detailed list of interposers, visit http://www.nexustechnology.com

Direct Attach Interposer

The direct attach interposer enables probing of all signals and is installed directly onto the target. The target must have mechanical clearance for the interposer. The use of the direct attach interposers is common for Package on Package (PoP) components.



Direct Attach interposer.

Technology	Package / Form factor
DDR3	Socketed – 78 Ball / 96 Ball Edge Probe – 78 Ball / 96 Ball Solder-down – 78 Ball / 96 Ball DIMM and SODIMM Interposer for MSO
LPDDR3	Socketed – 216 Ball / 211 Ball Solder-down – 178 Ball / 211 Ball

TDP7700 series TriMode probes for DDR3 measurements

The Tektronix TDP7700 Series TriMode probes are designed to meet DDR3 measurement challenges. The TDP7700 works with the 6 Series MSO, with full AC calibration of the probe and tip's signal path, to provide the highest probe fidelity available for real-time oscilloscopes. The innovative new probe design uses SiGe technology to provide the bandwidth and fidelity needed today and in the future.

TriMode probing lets one probe setup take differential, single ended, and common mode measurements accurately, increasing your efficiency. This unique capability lets you switch between differential, single ended and common mode measurements on the oscilloscope, without moving the probe's connection point.

A key TDP7700 connectivity innovation is using solder-down probe tips with the probe's input buffer mounted only a few millimeters from the tip. This approach provides unmatched usability for connecting to DDR3 circuits.

The TDP7708 probe with high impedance inputs and TriMode capability reduces the number of probes needed to take DDR3 measurements.

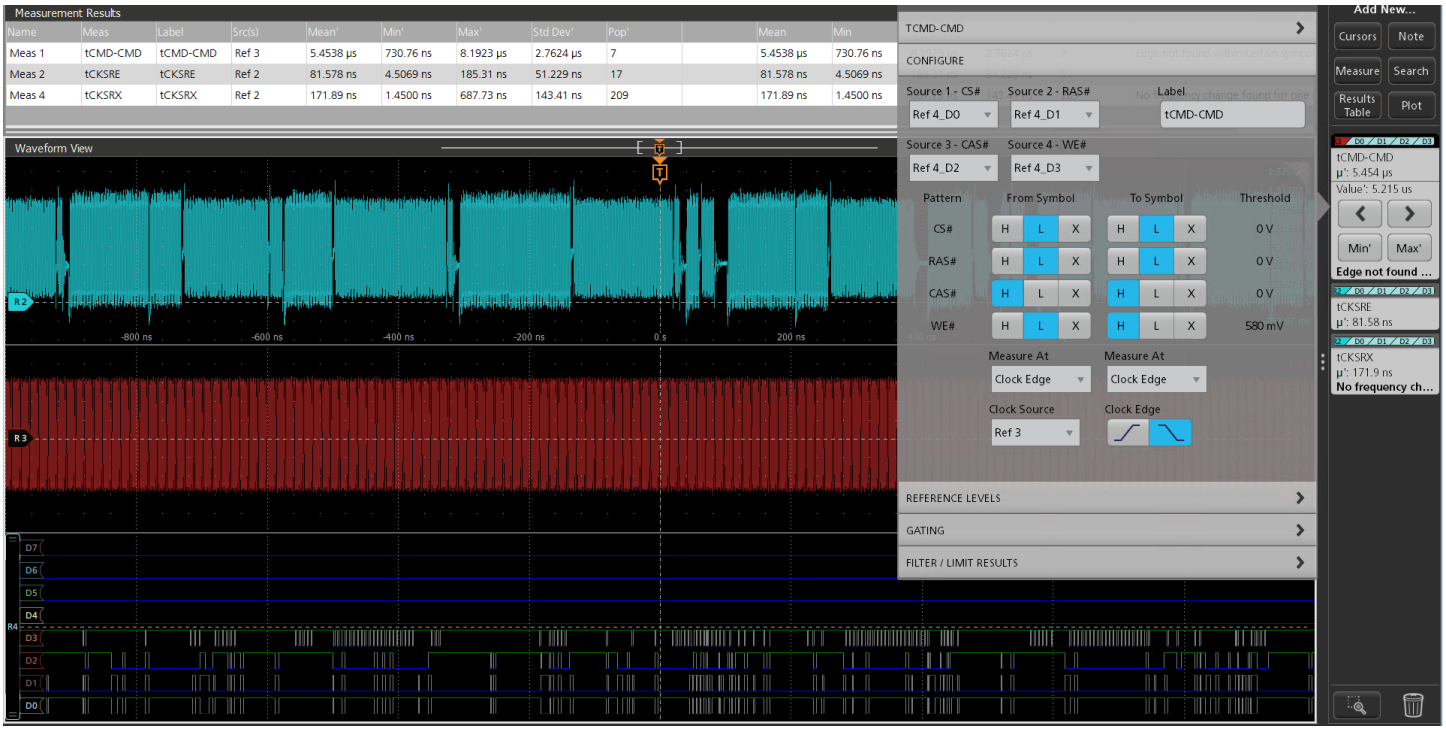
Other TDP7700 Series probe characteristics include:

- Excellent step response and low insertion loss up to 20 GHz
- Low-DUT loading with 100 kΩ (DC) and 0.4 pF (AC) performance
- High Common-Mode Rejection Ratio (CMRR)
- Low noise

TLP058 FlexChannel® logic probe for digital measurements

The 6 Series MSO provides digital channel capabilities to perform full protocol analysis of the entire memory bus. The TLP058 FlexChannel® logic probe connects the Tektronix 6 Series MSO to digital buses and signals on the device under test (DUT). The probe contains 8 data channels and connects the TLP058 logic probe to any FlexChannel oscilloscope input channel.

The TLP058 provides high performance digital inputs.



Configuring DDR3 digital measurements using TLP058 probes.

Specifications

- **Timing measurements**
  - **tRPRE** measures the width of the Read burst preamble. This is measured from the exit of tristate to the first driving edge of the differential strobe.
  - **tWPRE** measures the width of the Write burst preamble. It is measured from the exit of tristate to the first driving edge of the differential strobe.
  - **tPST** measures the width of Read or Write burst postamble. It is measured from the last falling edge crossing the mid reference level to the start of an undriven state (as measured by a rising trend per JEDEC specification).
  - **Hold Diff** measures the elapsed time between the designated edge of the single-ended waveform and the designated edge of a differential waveform. The measurement uses the closest single-ended waveform edge to the differential waveform edge that falls within the range limits.
  - **Setup Diff** measures the elapsed time between the designated edge of a single-ended waveform and when the differential waveform crosses its own voltage reference level. The measurement uses the closest single-ended waveform edge to the differential waveform edge that falls within the range limits.
  - **tCH(avg)** measures the average high pulse width calculated across a sliding 200 cycle window of consecutive high pulses.
  - **tCK(avg)** measures the average clock period across a sliding 200-cycle window.
  - **tCL(avg)** measures the average low pulse width calculated across a sliding 200 cycle window of consecutive low pulses.
  - **tCH(abs)** measures the high pulse width of the differential clock signal. It is the amount of time the waveform remains above the mid reference voltage level.
  - **tCL(abs)** measures the low pulse width of the differential clock signal. It is the amount of time the waveform remains below the mid reference voltage level.
  - **tJIT(duty)** measures the largest elapsed time between tCH and tCH(avg) or tCL and tCL(avg) for a 200-cycle window.
  - **tJIT(per)** measures the largest elapsed time between tCK and tCK(avg) for a 200-cycle sliding window.
  - **tJIT(cc)** measures the absolute difference in clock period between two consecutive clock cycles.
  - **tERR(n)** measures the cumulative error across multiple consecutive cycles from tCK(avg). It measures the time difference between the sum of clock period for a 200-cycle window to n times tCK(avg).
  - **tERR(m-n)** measures the cumulative error across multiple consecutive cycles from tCK(avg). It measures the time difference between the sum of clock periods for a 200-cycle window to n times tCK(avg).
  - **tDQSCK** measures the strobe output access time from differential clock. It is measured between the rising edge of clock before or after the differential strobe Read preamble time. The edge locations are determined by the mid-reference voltage levels.
  - t**CMD-CMD** measures the elapsed time between two logic states.
  - **tCKSRE** measures the valid clock cycles required after Self Refresh Entry (SRE) command. Changing the input clock frequency or the supply voltage is permissible only after tCKSRE time when the SRE command is registered.
  - **tCKSRX** measures the valid clock cycles required before the Self Refresh Exit (SRX) command. Changing the input clock frequency or the supply voltage is permissible provided the new clock frequency or supply voltage is stable for the tCKSRX time prior to SRX command.
- **Amplitude measurements**
  - **AOS** measures the total area of the signal above the specified reference level.
  - **AUS** measures the total area of the signal below the specified reference level.
  - **Vix(ac)** measures the differential input cross-point voltage measured from the actual crossover voltage and its complement signal to a designated reference voltage. This is measured on a single-ended signal.
  - **AOS Per tCK** measures the total area of the signal that crosses the specified reference level calculated over consecutive periods. It is applicable to clock and address/command waveforms only.
  - **AUS Per tCK** measures the total area of the signal that crosses the specified reference level calculated over consecutive periods. It is applicable to clock and address/command waveforms only.
  - **AOS Per UI** measures the total area of the signal that crosses the specified reference level calculated over consecutive unit intervals. It is applicable to data and data strobe waveforms only.
  - **AUS Per UI** measures the total area of the signal that crosses the specified reference level calculated over consecutive unit intervals. It is applicable to data and data strobe waveforms only.

Additional details

Details	DDR3	LPDDR3
Speed (MT/s)	800, 1066, 1333, 1600, 1866, and 2133	333, 800, 1066, 1200, 1333, 1466, 1600, 1866 and 2133
Max slew rate	10 V/ns	8 V/ns
Typical V swing	1 V	0.6 V
20-80 risetime	60 ps	45 ps
Report	HTML and PDF format	
Source support	Live analog signals, reference waveforms, and math waveforms	
De-embedding support	Filter file using math subsystem	

Ordering information

Required hardware

Oscilloscope	6 Series MSO oscilloscope with minimum bandwidth of 4 GHz (6-BW-4000) for debug and a recommended bandwidth of 8 GHz (6-BW-8000) for DDR3/LPDDR3 automated conformance testing.
Operating system	6-WIN (removable SSD with Microsoft Windows 10 operating system). Optional - Required only for DDR3/LPDDR3 automated conformance testing

Required software

Application	Options	License type
DDR3 and LPDDR3 Automated Compliance Solution for 6 Series MSO [2]	6-CMDDR3	New instrument license
	SUP6-CMDDR3	Upgrade license
	SUP6-CMDDR3-FL	Floating license [3]
DDR3 and LPDDR3 Analysis and Debug Solution for 6 Series MSO [4]	6-DBDDR3	New instrument license
	SUP6-DBDDR3	Upgrade license
	SUP6-DBDDR3-FL	Floating license [3]

Recommended probes and accessories

Recommended probes

Accessory type	Quantity
TDP7708 Tri-mode probe with P77STFLXB adapters	Two probes are required for testing a DUT with DQ and DQS. Three probes are required for testing a DUT with DQ, DQS and clock.
TLP058	One probe is required for probing CS, RAS, CAS, and WE lines.
TDP3500	One probe is required for CS as Analog signal.

Recommended test fixtures

Accessory type	Vendor
DDR3: x4, x8, 16 socketed, solder-down and direct attach interposers	Sold through Tektronix and Nexus Technologies [5]
LPDDR3: BGA and PoP interposers	

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

Product Area Assessed: The planning, design/development and manufacture of electronic Test and Measurement instruments.

2 DDR3 and LPDDR3 Automated Compliance Solution for 6 Series MSO requires 6-DBDDR3 and 6-DJA as a pre-requisite for running DDR and Eye diagram measurements.

3 Floating licenses are transferrable from any 6 Series MSO to any other 6 Series MSO, for use of one instrument at a time.

4 Additional information about DDR analysis is available at https://www.tek.com/ddr-test-validation-and-debug.

5 Contact your local Tektronix representative for details.

ASEAN / Australasia (65) 6356 3900
Belgium 00800 2255 4835*
Central East Europe and the Baltics +41 52 675 3777
Finland +41 52 675 3777
Hong Kong 400 820 5835
Japan 81 (3) 6714 3086
Middle East, Asia, and North Africa +41 52 675 3777
People's Republic of China 400 820 5835
Republic of Korea +822 6917 5084, 822 6917 5080
Spain 00800 2255 4835*
Taiwan 886 (2) 2656 6688

Austria 00800 2255 4835*
Brazil +55 (11) 3759 7627
Central Europe & Greece +41 52 675 3777
France 00800 2255 4835*
India 000 800 650 1835
Luxembourg +41 52 675 3777
The Netherlands 00800 2255 4835*
Poland +41 52 675 3777
Russia & CIS +7 (495) 6647564
Sweden 00800 2255 4835*
United Kingdom & Ireland 00800 2255 4835*

Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777
Canada 1 800 833 9200
Denmark +45 80 88 1401
Germany 00800 2255 4835*
Italy 00800 2255 4835*
Mexico, Central/South America & Caribbean 52 (55) 56 04 50 90
Norway 800 16098
Portugal 80 08 12370
South Africa +41 52 675 3777
Switzerland 00800 2255 4835*
USA 1 800 833 9200

* European toll-free number. If not accessible, call: +41 52 675 3777

For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tek.com.

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