

80A07
Electrical Clock Recovery Instrument
User Manual



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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Power Disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this Manual

These terms may appear in this manual:



WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*



CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and Terms on the Product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:



Environmental Considerations

This section provides information about the environmental impact of the product.

Product End-of-Life Handling

Observe the following guidelines when recycling an instrument or component:

Equipment Recycling. Production of this equipment required the extraction and use of natural resources. The equipment may contain substances that could be harmful to the environment or human health if improperly handled at the product's end of life. In order to avoid release of such substances into the environment and to reduce the use of natural resources, we encourage you to recycle this product in an appropriate system that will ensure that most of the materials are reused or recycled appropriately.



The symbol shown to the left indicates that this product complies with the European Union's requirements according to Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). For information about recycling options, check the Support/Service section of the Tektronix Web site (www.tektronix.com).

Restriction of Hazardous Substances

This product has been classified as Monitoring and Control equipment, and is outside the scope of the 2002/95/EC RoHS Directive. This product is known to contain lead, cadmium, and hexavalent chromium.

Preface

This is the user manual for the 80A07 Electrical Clock Recovery instrument. The manual covers capabilities, installation, operation, and specifications of the instrument.

Manual Structure

This manual is composed of the following chapters:

- *Getting Started* provides a brief product description and how to install your instrument. Information about accessories to use with your product is also found here.
- *Reference* provides more detail on the functions and capabilities of the instrument.
- *Specifications* lists the specifications for this instrument.

Getting Started

This section contains information on key features of your instrument, installing your instrument, and getting acquainted with the controls.

Clock Recovery

Many communication standards now specify that jitter testing must be carried out using a reference clock that has been derived from the data signal. Typical phase lock loop (PLL) characteristics are specified in terms of the -3 dB bandwidth of the recovery loop, the rate of rolloff of the frequency response, and the degree of response peaking allowable.

The 80A07 measures and displays the PLL frequency response from 100 kHz to 12 MHz. The 80A07 allows full control of parameters including loop bandwidth (LBW), peaking/damping and rolloff.

Design and test engineers can now find and lock onto signals of undefined or unknown data rates. The engineer can recover full-rate clocks, including spread spectrum clocks, for signals at data rates from 100 Mb/s to 12.5 Gb/s. The engineer has full control of key parameters for variable-loop bandwidth, peaking/damping and first and second order rolloffs, optimizing jitter tracking.

Golden PLL

Many test standards require the use of a Golden PLL (phase lock loop.) To assure repeatability, most serial data compliance test standards specify the PLL characteristics for jitter measurement. Each standard provides an optimum LBW setting for clock recovery, often called the Golden PLL.

Recover Clocks for Optical Storage, Enterprise and Telecom Testing

The 80A07 has been designed to provide users with flexibility and accuracy in compliance measurements. It is ideal for optical test applications, like 4x/8x Fibre Channel and 10G Ethernet standards, where the signal under test must be split off and converted from optical to electrical before being fed into the clock recovery data input. The 80A07 recovers a full-rate clock up to 12.5 Gb/s, an important requirement for testing XFP and other 10 Gb/s MSA modules.

Key Features

The 80A07 provides a quality clock recovery solution with the following features:

- 100 Mb/s to 12.5 Gb/s continuous data rate coverage
- Accurate variable loop bandwidth from 100 kHz to 12 MHz
- Auto lock capability with LED display
- Programmable peaking adjustment with first and second order rolloff capability
- Self-measured and displayed (Phase Locked Loop) PLL frequency response
- USB control connection or stand- alone operation via front panel
- Single-ended or differential 50 Ω data inputs/outputs
- DC coupled data through path
- Full and divided clock outputs with selectable divide ratios
- Measurement of clock phase deviation as a function of frequency and time
- Data measurement capability
 - Edge Density Measurement determines the mark density of the signal under test
- Ideal for spread spectrum clock (SSC) applications with large frequency excursions
- Four memory locations for saving user setups

Installation

To install the 80A07, connect the supplied AC power cord to a properly grounded AC supply. The input voltage requirement is 100 VAC to 240 VAC at 50 Hz to 60 Hz.

Press the power button on the instrument using the front-panel On/Standby switch.

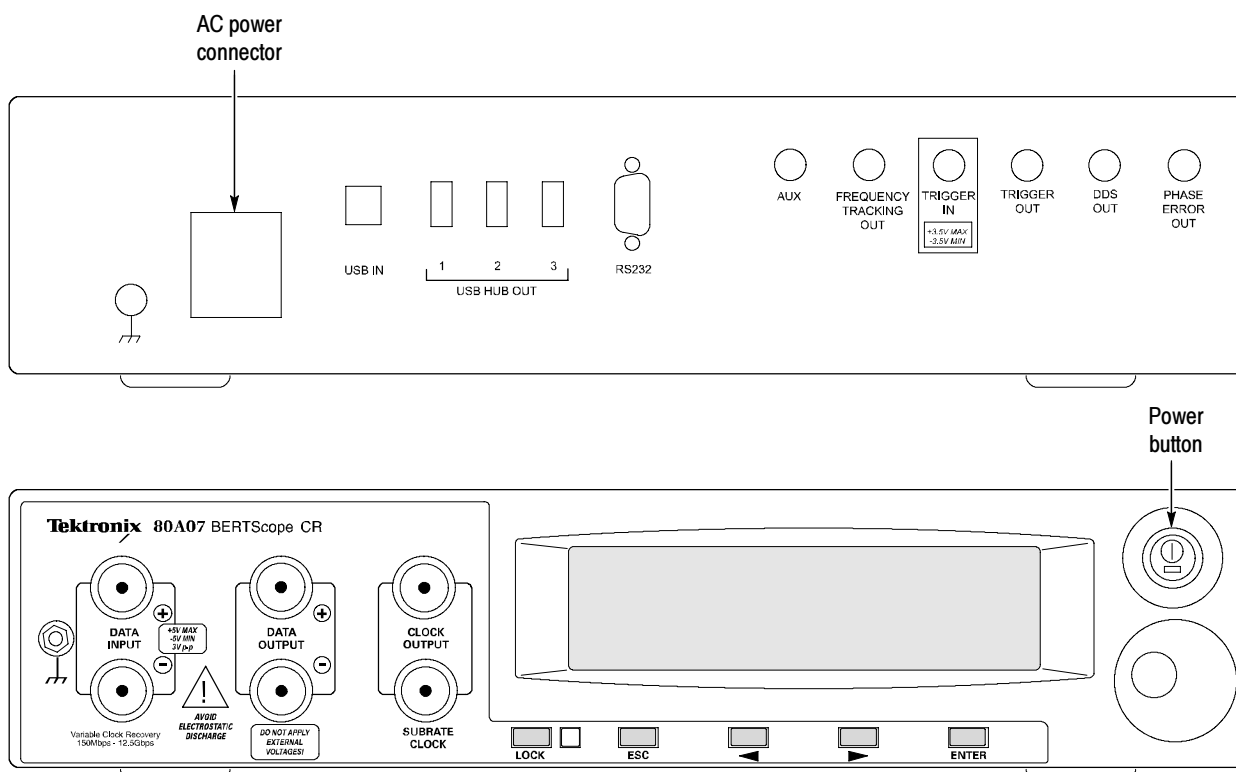


Figure 1: Installation

Electrostatic Discharge

To prevent electrostatic damage, follow the precautions described in this manual and in the documentation provided with any connecting instruments.

Circuitry in the instrument is very susceptible to damage from electrostatic discharge or from overdrive signals. Be sure to only operate in a static-controlled environment. Be sure to discharge to ground any electrostatic charge that may be present on the center and outer connectors of cables before attaching the cables.

Know your signal source. If it is capable of delivering overvoltages, it is safer to not depend on the signal source settings for protection, but instead use an external attenuator that protects the input from the worst-case conditions. For example, for a 10 V maximum source connected to a 1 V maximum input, use a 10X attenuator. Where possible, connect your cables to the signal source first, and to the instrument second.



CAUTION. *To prevent damage from electrostatic discharge, install the 50 Ω terminations on the I/O connectors when the connectors are not in use.*

To prevent damage to the instrument, discharge to ground any electrostatic charge that may be present on the center and outer conductors of cables before attaching the cables to the instrument.

To prevent damage to the instrument, do not create an ESD antenna by leaving cables dangling off the input with the other end open.

Always use a wrist strap when making signal connections. Wear antistatic clothing and work in a static-free workstation.



To prevent damage to the instrument, do not apply a signal outside the Maximum Input Voltage Swing.

Static-Controlled Workstation

For information on creating a static-controlled workstation, consult the Electronic Industries Association document, *EIA-625; Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices*.

Getting Acquainted with Your Instrument

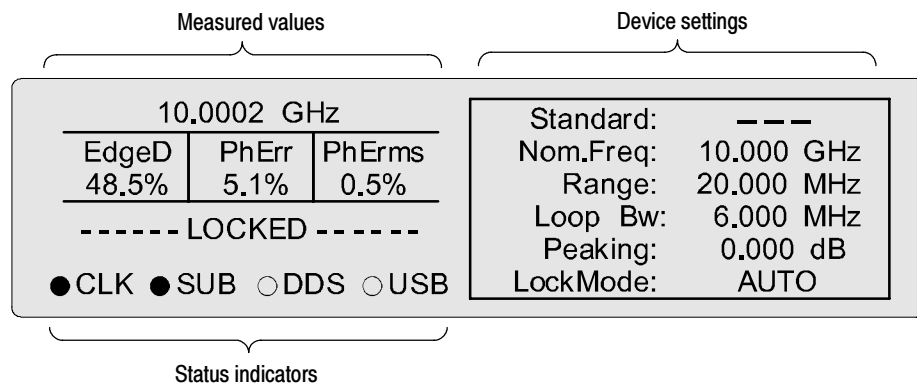
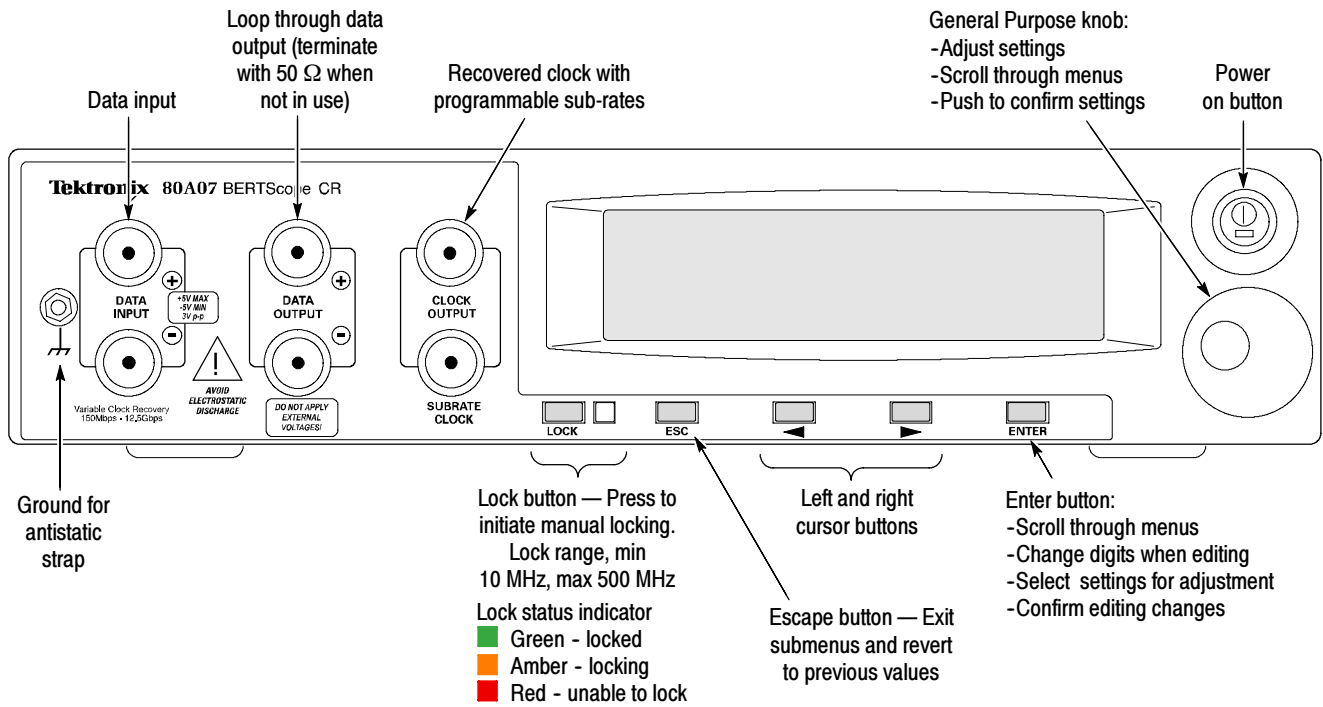


Figure 2: 80A07 front panel and display

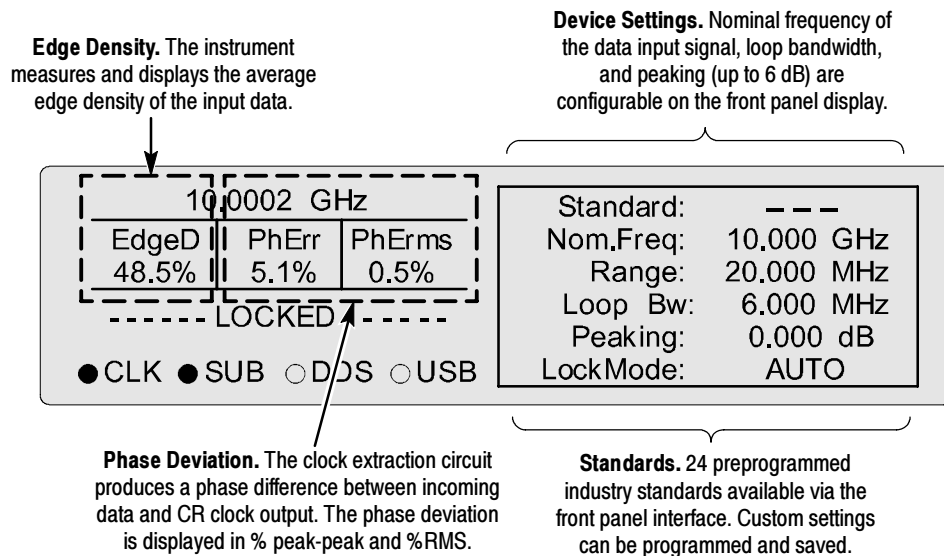


Figure 3: 80A07 display details

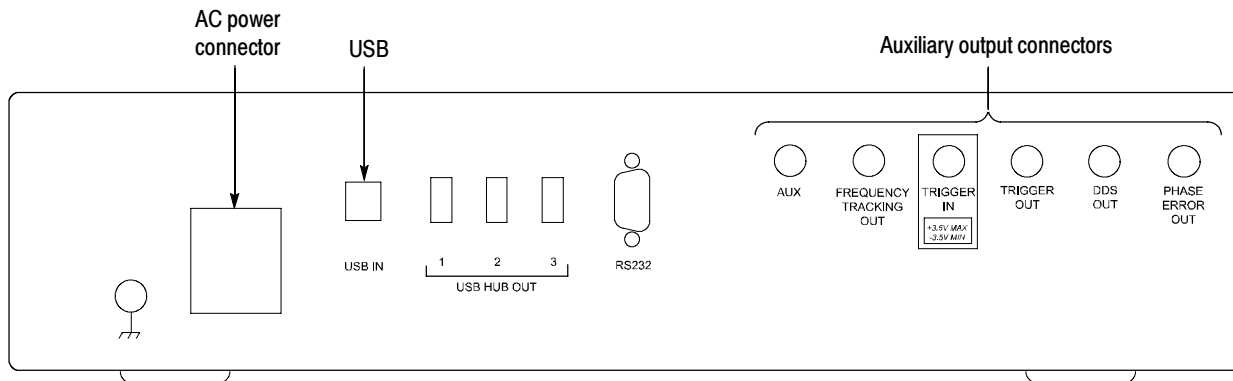


Figure 4: 80A07 rear panel

Input and Output Connector Care

The input and output connectors on the front panel are highly sensitive connectors providing high-frequency signal connections. To maintain signal integrity, it is important not to damage these connectors.

Never attach a cable to a connector if the cable has a worn or damaged connector because you may damage the connector. When attaching or removing a cable from the connectors, align the connectors carefully before turning the nut. Then turn only the nut, not the cable. Use light finger pressure to make the initial connection, then tighten the nut lightly with a wrench.



CAUTION. To prevent electrostatic damage to the 80A07 and other instrumentation, follow the precautions described in this manual and in the documentation provided with any connecting instruments. (See Electrostatic Discharge starting on page 3.)

NOTE. For best repeatability and to prolong connector life, use a torque wrench, and tighten the connection to the range of 79-112 N·cm (7-10 in lb).

If the connectors receive heavy use, such as in a production environment, you should install adapters to make connections.

Setting up the 80A07

After the proper connections have been made for data input and clock out, and the instrument has been powered on, you may adjust the input settings.

NOTE. The *DATA OUTPUT* connectors must be terminated if not in use, or else the reflections that result will severely degrade performance.

Current settings are displayed on the right side of the display. Use the knob or cursor buttons to scroll through menu items. Press the knob or enter button to select an item to adjust. Use the **ESC** button to back out of a menu or cancel an adjustment. When editing a numeric setting, use the left and right cursor buttons to move through digits and use the knob to make changes. Press the knob or **ENTER** button to accept a change, or press the **ESC** button to cancel changes.

Many industry standards are also available from the front panel menu. After selecting a standard, the nominal data rate, loop bandwidth and peaking settings are entered automatically.

You can manually enter the following settings:

- | | |
|------------------------|--|
| ■ Nominal Data Rate | Nominal rate of the recovered clock. |
| ■ Lock Range | The frequency range around the nominal rate that will be scanned during locking. |
| ■ Bandwidth | Bandwidth of the recovery loop measured at -3 dB. |
| ■ Peaking | Peaking of the recovery loop. Also sets 1st or 2nd order roll-off of untracked jitter. |
| ■ Nominal Edge Density | Expected edge density of incoming data. Required to set bandwidth correctly. |

- Edge Density Mode Sets bandwidth. Calculations are based on the Expected Edge Density (user entered) or edge density measured during lock.
- Clock Amplitude Output amplitude of the full-rate clock.
- Sub-rate Amplitude Output amplitude of the sub-rate clock.
- Sub-rate Division Division ratio of the sub-rate clock.

All settings are saved automatically at power off and restored at power on. You can also save current settings to one of four Setups that can be recalled later.

The left side of the display provides several continuously updated measurements:

- Frequency The measured frequency of the recovered clock.
- Phase Error The peak-to-peak phase error between the incoming data and the recovered clock. This measured value increases if jitter is present on the input data that is not being tracked by the recovered clock.
- Phase Error RMS The RMS phase error between the incoming data and the recovered clock.
- Lock State Reports whether the CR is locked, unlocked, or in the process of locking.

By default, the 80A07 is configured in Auto Lock Mode, where it automatically attempts to acquire lock if the detected Phase Error exceeds the Phase Error Limit setting or if the recovered clock is unstable. The user may force a relock at any time by pressing the Lock button.

You can utilize the 80A07 with a Tektronix sampling oscilloscope such as the DSA8200 Digital Serial Analyzer, to display the data input. Use the clock output to trigger the oscilloscope. Figure 5 shows a typical setup configuration.

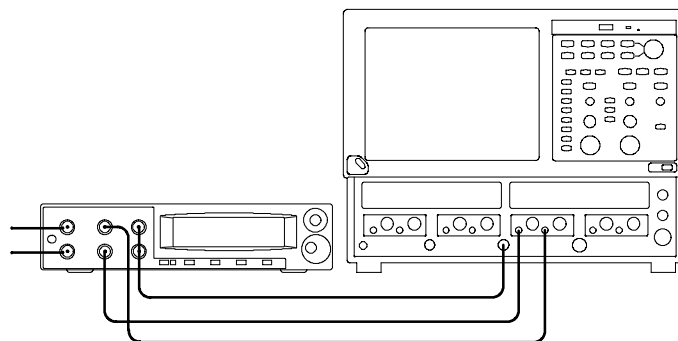


Figure 5: Typical setup configuration

Remote Interface

The 80A07 can be remotely controlled via the virtual front panel software. The virtual front panel software can be installed on a personal computer or a Tektronix sampling oscilloscope. Connection to the 80A07 is made through the USB interface. The virtual front panel software requires the Microsoft Windows 2000 or XP operating system.

The virtual front panel software is provided on the CDROM included with your instrument. Insert the CDROM into the CDROM drive and follow the installation prompts. Refer to the user instructions on the CDROM for operation of the virtual front panel software.

Remote Control

Remote control of the 80A07 is possible with the use of the Software Developer's Kit (SDK). The SDK is available on the CDROM provided with your instrument. Refer to the instructions provided on the CDROM for use of the developer's kit.

User Adjustments

The 80A07 contains no user adjustments.

Accessories

This section lists the standard and optional accessories available for the instrument.

Standard Accessories

The following accessories are shipped with the instrument:

Table 1: Standard accessories

Item	Part number
80A07 Electrical Clock Recovery User Manual	071-2195-xx
80A07 Software disc (Virtual Front Panel and software developer's kit)	063-4040-xx
Power Cord	161-0104-xx
Rack mount hardware	
Left bracket	119-7360-xx
Right bracket	119-7361-xx
Hardware bag (screws)	119-7363-xx
USB cable	174-4401-xx
Fuse	119-7362-xx

Optional Accessories

You can order the following accessories for use with the 80A07. Consult a current Tektronix catalog for additions, changes, and details:

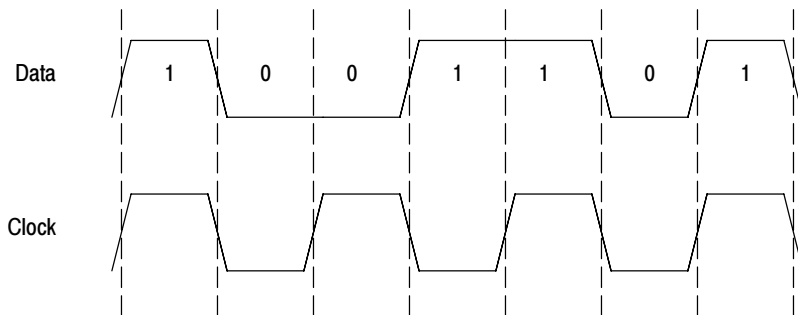
Table 2: Optional accessories

Item	Part number
Cables (450 mm/18 inch; 1 dB loss @ 20 GHz) recommended for work to 20 GHz.	015-0560-xx
SMA male 50 Ω termination	015-1022-xx
Connector saver, 3.5 mm SMA	015-0549-xx
SMA accessory kit	020-1693-xx

Reference

Clock Recovery Basics

A clock recovery system is used to generate a sampling clock from a stream of data with an embedded clock. The sampling clock is then used by the decision circuit to determine when to decide the logic state of the incoming data. In most cases, the data is line coded in a format referred to as “Non-Return to Zero” (NRZ). As the name implies, the logic state in NRZ data remains constant when the data contains a series of bits with the same value, 1 or 0.

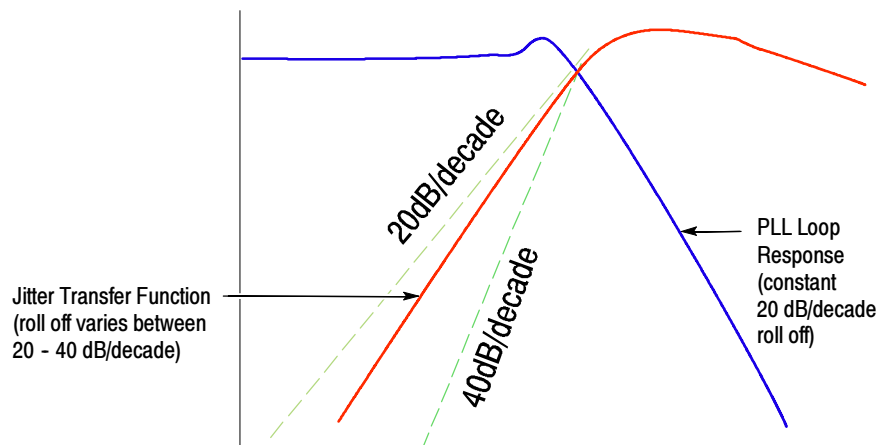


Jitter Transfer

The clock recovery PLL (phased lock loop) removes virtually all of the low frequency jitter from the input data and none of the very high frequency jitter components. Periodic jitter with frequency components near the roll slope of the PLL loop response will be attenuated by some degree. The Jitter Transfer Function is a plot of the attenuation of the jitter passing from the input data to the recovered clock output as a function of frequency content.

Loop Response Peaking

The Jitter Transfer Function is not exactly an inverse of the PLL loop frequency response. The slope of the jitter transfer function, as well as its peaking will often be different that of the PLL loop response.



The parameters which determine the JTF roll off slope and peaking are the relationship between loop bandwidth and the bit rate, and the amount of peaking in the PLL response. Several examples of the jitter transfer function versus PLL loop response can be seen in the next section.

The 80A07 has the ability to measure the PLL response and the jitter transfer function and display a plot of these to the user. This can be useful to understand the relationship of these parameters at the particular data rate.

Golden PLL Many test standards require the use of a Golden PLL (phase lock loop.)

The 80A07 is an instrumentation grade clock recovery system. The PLL parameters of clock frequency, loop bandwidth and peaking are accurately calibrated, and adjustable by the user. This is useful in two situations — during transmitter testing when the user wants to measure parameters in the data signal through the channel exactly as the receiver would, and for standards compliance testing.

Because the clock recovery system removes the low frequency jitter from the regenerated clock, the loop parameters must be calibrated and set to known values for repeatable jitter measurements. To assure repeatability, most serial data compliance test standards specify the PLL characteristics for jitter measurement. A PLL which is set to these specified parameters is often referred to as a “Golden PLL”.

Edge Density The logic state of NRZ data does not change between successive bits of the same logic state. Therefore, there will not be a logic edge in every bit time slot, or Unit Interval. The edge density refers to the average percentage of unit intervals which contain a transition. A repeating 1010 pattern has a transition occurring during every unit interval, and therefore an edge density of 100%. A Pseudo Random Bit Stream (PRBS) pattern has an edge density of 50%. Other examples

include a repeating 1100 pattern, which has a 50% edge density, and a repeating 11110000 pattern, which would have an edge density of 25%.

All clock recovery systems require a minimum edge density to operate properly. If a long pattern of all ones or zeros were sent, the clock recovery would not be able to track jitter or spread spectrum clock (SSC) modulation or may even lose lock on the data clock. Data encoding standards eliminate this possibility by either modulating the bit stream using a set of rules that set a minimum for the number of consecutive bits set to the same logic state, or add overhead data bits to the packet which guarantee transitions occur even when the payload data is bit stream of only one logic state.

The edge density represents the amount of energy going into the clock recovery phase lock loop. The average energy effects the parameters of loop gain and bandwidth. Therefore, an instrumentation grade clock recovery system such as the 80A07 requires information on the edge density to keep the loop parameter settings calibrated. In the 80A07, this can be done by one of two methods, auto and manual modes. In auto mode, the actual average edge density is measured and automatically calibrates the loop parameter settings. In manual mode, the user enters the expected edge density. A warning message is generated when the measured edge density varies greatly from the expected edge density. Some serial data compliance standards, such as SATA, require the loop parameters be calibrated to a specified edge density, regardless of the edge density of the actual data.

Clock Multiplication and Division

To lock to NRZ data, the phase detector used in a clock recovery PLL does not require an edge at every unit interval. This property can be utilized to multiply a clock frequency. The PLL will lock to a frequency that is a multiple of the clock applied to the data input.

To multiply a clock, you enter the desired output frequency as the clock frequency. This must be an integer multiple of the input frequency. To calibrate the loop response (for known jitter transfer performance), you also enter the preclinical of the multiplication factor in percent as the expected edge density. For example, for 2X multiplication, enter 50 %, for 3x enter 33 %, for 5x enter 20 % etc. The clock recovery unit will phase lock to the multiple of the input data frequency, providing a clean multiple of the input clock at the output.

While the PLL can accept data with edges at a sub-multiple of the clock rate, it can handle the converse - edge rates greater than one per unit interval (corresponding to edge densities greater than 100%). Thus, the PLL itself can not be used directly to divide a clock to a lower multiple.

The 80A07 provides an additional Sub-Rate Clock output which is divided to a sub multiple of the main clock output. The 80A07 utilizes a user programmable divider for this purpose. The divider is specifically designed to minimize the addition of jitter to the recovered clock signal. This sub-rate clock output can be used to precisely divide a clock down to a sub multiple frequency. The 80A07

provides a large selection of division ratios, ranging from 1 to 648. To use the clock recovery instrument as a precision clock divider, you would set the clock frequency to the actual input frequency and the edge density to 100%. Then, select the desired division ratio for the SUBRATE CLOCK output.

Note that because the divider circuits are located outside of the PLL, the calibrated loop characteristics and jitter transfer function will scale in frequency by the sub-rate divisor.

User Interface

The 80A07 can be used in standalone operation or in conjunction with a Tektronix sampling oscilloscope.

As a standalone instrument, information is always immediately available on the front panel display, showing parameters such as the PLL bandwidth, lock status, bit rate, peaking and rolloff.

For easy verification of compliance, the correct characteristics are automatically set when a given standard is selected from a pull-down menu. However, full control of parameters is possible with direct entry of the user parameters. The 80A07 has variable jitter peaking, allowing jitter gain in excess of 10 dB if desired.

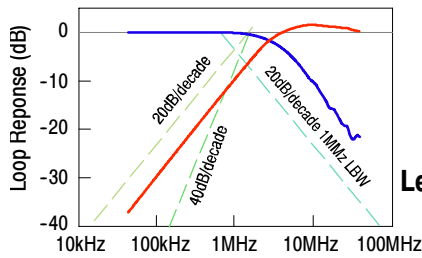
Remote control of the instrument is supported via USB and a software developer's kit.

The 80A07 instrument provides a solution for triggering a DSA8200, CSA8000, and TDS8000 Series instruments from single-ended or differential electrical signals. The 80A07 can be used as a standalone clock recovery device or in conjunction with the following Tektronix sampling oscilloscopes:

- DSA8200 Digital Serial Analyzer
- CSA8000, CSA8000B, and CSA8200 Communications Signal Analyzer (With product software version 2.0 or later)
- TDS8000, TDS8000B, and TDS8200 Digital Sampling Oscilloscope (With product software version 2.0 or later)

Standards Coverage

The following graphics show compliance settings, and the accompanying table (Table 3) show common standards, the data rates they employ, and the loop bandwidths required for compliance measurements.



Blue trace: Jitter Transfer Function (roll off varies between 20 - 40 dB/decade)

Red trace: PLL Loop Response (constant 20 dB/decade roll off)

Legend

<p>10 Gigabit Ethernet Bit Rate: 10.3125 Gb/s Loop Bandwidth: 4 MHz Peaking: 0 dB</p>	<p>XAUI Bit Rate: 3.125 Gb/s Loop Bandwidth: 1.875 MHz Peaking: 0 dB</p>	<p>2x Fibre Channel Bit Rate: 2.12 Gb/s Loop Bandwidth: 1.275 MHz Peaking: 0.3 dB max</p>	<p>4x Fibre Channel Bit Rate: 4.25 Gb/s Loop Bandwidth: 2.55 MHz Peaking: 0.3 dB max</p>
<p>8x Fibre Channel Bit Rate: 8.5 Gb/s Loop Bandwidth: 5.1 MHz Peaking: 0.3 dB max</p>	<p>8x OIF CEI 6G+ Bit Rate: 6.25 Gb/s Loop Bandwidth: 3.6 MHz Peaking: 0.1 dB max</p>	<p>OIF CEI 11G+ Bit Rate: 11.0 Gb/s Loop Bandwidth: 4 MHz Peaking: 0.1 dB max</p>	<p>OIF CEI 11G+ Bit Rate: 11.0 Gb/s Loop Bandwidth: 6 MHz Peaking: 0.1 dB max</p>
<p>OIF CEI 11G+ Bit Rate: 11.0 Gb/s Loop Bandwidth: 8 MHz Peaking: 0.1 dB max</p>	<p>Serial ATA Gen 2 $f_{\text{baud}}/500$ Bit Rate: 3.0 Gb/s Loop Bandwidth: 6 MHz Peaking: 2.1 dB</p>	<p>Serial ATA Gen 2 $f_{\text{baud}}/1667$ Bit Rate: 3.0 Gb/s Loop Bandwidth: 0.9 MHz Peaking: 0 dB</p>	<p>SONET OC-48/SDH STM-16 Bit Rate: 2.488 Gb/s Loop Bandwidth: 1 MHz Peaking: 0 dB</p>
<p>SONET OC-192/SDH STM-64 Bit Rate: 9.95 Gb/s Loop Bandwidth: 4 MHz Peaking: 0 dB</p>	<p>XFP/XFI Bit Rate: 10.5 Gb/s Loop Bandwidth: 8 MHz Peaking: 0.1 dB max</p>	<p>Fully Buffered DIMM II Bit Rate: 6.4 Gb/s Loop Bandwidth: 11 MHz Peaking: 0.5 dB</p>	<p>PCI Express II Bit Rate: 5.0 Gb/s Loop Bandwidth: 5 MHz Peaking: 1 dB max</p>

Table 3: Standards supported

Standard		Data Rate (Gb/s)	Common Clock Divide Ratios	Loop Bandwidth (MHz)	Peaking (dB)	Slope	Spread Spectrum Clocking	
Ethernet	1.0			0.637				
	10Gb/s Ethernet Transmitter Test	10.312		≤ 4		-20 dB/decade	No	
	XAU1	3.125		1.875				
Fibre Channel	1X	1.063	10	0.638	0.3 max	-20 dB/decade	No	
	2X	2.12	20	1.275	0.3 max			
	4X	4.25	40	2.550	0.3 max			
	8X	8.5	80	5.100	0.3 max			
OIF CE1 ¹	6+Gb/s	4.976 to 6.375		3.6 ($f_{\text{baud}}/1667$)	0.1 max	-20 dB/decade	No	
	11+Gb/s	9.95 to 11.1		8, ITU 6 ($f_{\text{baud}}/1667$) other				
SATA ²	Gen 1	250UI	1.5	15	6.000		Yes	
		$f_{\text{baud}}/1667$			0.900	2.09 - 1.25 dB		Type 2
		5UI			300.000			
	Gen 2	$f_{\text{baud}}/500$	3	30	6.000	2.09 - 1.25 dB		Type 2
		$f_{\text{baud}}/1667$			1.800	2.09 - 1.25 dB		Type 2
		$f_{\text{baud}}/10$			300.000	2.09 - 1.25 dB		Type 2
SONET/SDH	OC12/STM-4	0.622		0.250		-20 dB/decade	No	
	OC48/STM-16	2.488		1.000				
	OC192/STM-64	9.95		4.000				
XFP/XFI	XFP/XFI	Receiver Test	9.95 - 11.2	64	8.000	0.1 max	No	
		Transmitter Test			4.000	0.1 max		-20 dB/decade
Fully Buffered DIMM	FB-DIMM1	3.2, 4.0	24	11 to 33	0.5 to 3	2nd Order	Yes. Transmitter Test: Full SSC swing. Receiver Test: 0.06 UI swing.	
		4.8	24	11 to 22				
	FB-DIMM2	4.8, 6.4, 8.0, 9.6	Forwarded Clock	11 to 22	0.5 to 2			

Table 3: Standards supported (cont.)

Standard		Data Rate (Gb/s)	Common Clock Divide Ratios	Loop Bandwidth (MHz)	Peaking (dB)	Slope	Spread Spectrum Clocking
PCI Express	I	2.5	25	1.500		1st order with -20 dB/decade	Yes, Optional. Receiver Test: 65 ps pk-pk swing
	II	5	50	5 to 16 8 to 16	Up to 1 dB Up to 3 dB	1st or 2nd order	
SAS ³	Gen 1	$f_{\text{baud}}/1667$	1.5	15	0.900	1st order (single pole)	
	Gen 2	$f_{\text{baud}}/1667$	3	30	1.800	1st order (single pole)	

¹ 8 MHz for most tests for ITU applications, BW/1667 other. Minimum of 4 MHz for stress testing in one case.

² Gen 1 & 2 categories: “i” (internal, hard drives etc.) and “m” (medium reach) use $f_{\text{baud}}/500$ and $f_{\text{baud}}/10$ for Gen 2 and 250UI and 5UI for Gen 1.

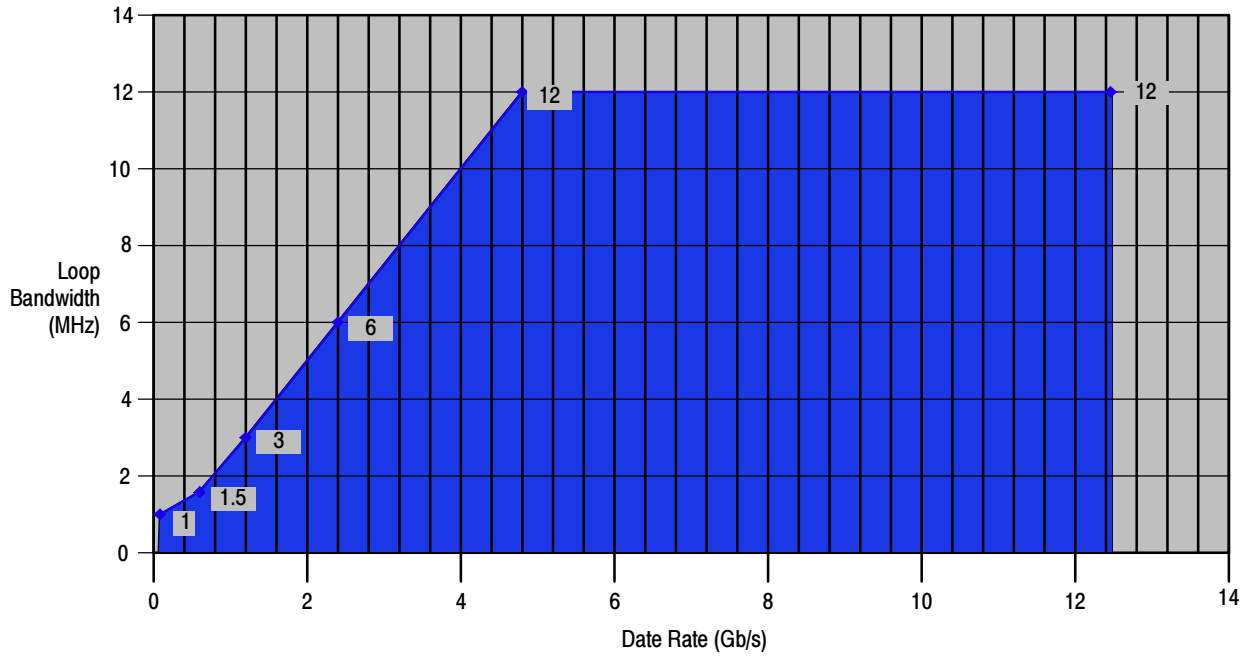
“x” (extended reach) uses $f_{\text{baud}}/1667$, Type 2.

Peaking bandwidths Implied: specified as damping factor of 0.707 min to 1.00 max — conversion taken from Gardner.

Loop bandwidths specified with transition density of 1 (100% or 1010101 pattern). Assumption is that loop bandwidth will change proportionally as transition density reduces.

³ Specified as damping factor of 0.707 min to 1.00 max — conversion taken from Gardner.

Loop bandwidths specified with transition density of 1 (100% or 1010101 pattern). Assumption is that loop bandwidth will change proportionally as transition density reduces.



The 80A07 has a variable loop bandwidth from 100 kHz to 12 MHz. The calibrated loop bandwidth is limited as indicated by the graph.

Figure 6: Clock recovery loop bandwidth versus data rate

Specifications

Electrical Sampling Modules

This section contains specifications for the 80A07 Electrical Clock Recovery instrument.

To meet specifications, two conditions must first be met:

- The instrument must have been operating continuously for 20 minutes within the operating temperature range specified.
- The instrument must be in an environment with temperature, altitude, and humidity within the operating limits described in these specifications

Table 4: Characteristics

Specifications	Characteristics
Data inputs / outputs	
Input configuration	True differential
Output configuration	True differential Unused outputs must be terminated into 50 Ω .
Connector type	APC 3.5
Impedance	50 Ω
Coupling	DC
Insertion loss	-2.6 dB or better 10 MHz to 12.5 GHz
Maximum nondestruct range	5 V _{pk-pk}
Maximum operating range	5 V _{pk-pk}
Input sensitivity	
Single ended	30 mV _{pp} at 10 Gbps
Differential	15 mV _{pp} at 10 Gbps
Clock output	
Connector type	APC 3.5
Impedance	50 Ω
Coupling	DC
Amplitude	
Minimum	300 mV _{pp}
Typical	540 mV _{pp}

Table 4: Characteristics (cont.)

Specifications	Characteristics
Amplitude accuracy	10% or 30 mV
Duty cycle accuracy	3% UI
Jitter	RMS, at 800 mV _{pp} input, 10 Gps, 1010 pattern, 2 MHz BW, 0.5 dB peaking
Typical	70 fsec
Maximum	250 fsec
Return Loss	-15 dB minimum
Rise/Fall	80/20% point measurements
Typical	25 ps
Maximum	30 ps
Substrate output	
Connector type	APC 3.5
Impedance	50 Ω
Coupling	DC
Divider function from main CLOCK OUTPUT	Full rate divided by 1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 25, 28, 30, 32, 35, 36, 40, 42, 45, 48, 49, 50, 54, 56, 60, 63, 64, 70, 72, 80, 81, 90, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648. Odd division ratios have non-50% duty cycles.
Amplitude	Adjustable
Minimum	250 mV _{pp}
Maximum	900 mV _{pp}
Amplitude accuracy	10% or 30 mV Measured at div by 1, typically ± 25% for all division ratios
Duty cycle accuracy	5% UI Measured at div by 1 2 4 8 16 32 64 128
Jitter	RMS, at divide-by-1, 800 mV _{pp} input, 10 Gps, 1010 pattern, 2 MHz BW, 0.5 dB peaking.
Typical	70 fs
Maximum	250 fs
Return loss	
Minimum	-15 dB 100 KHz to 12.5 GHz
Rise/fall	80/20% point measurements, divide-by-1
Typical	25 ps
Maximum	30 ps

Table 4: Characteristics (cont.)

Specifications	Characteristics
Control interface	
Type	USB 2.0
Uplink ports	1
Additional ports	3
Clock recovery response	
Loop bandwidth	Refer to graph for allowable data rate versus loop bandwidth combination settings, Adjustable
Minimum	100 KHz
Maximum	12 MHz
Frequency rolloff	Adjustment of peaking also adjusts the frequency switchover point between low-frequency -40 dB/decade rolloff rate and high-frequency -20 dB/decade rolloff rate.
Minimum	20 dB/dec
Maximum	40 dB/dec
Peaking	Adjustable
Minimum	0 dB
Maximum	6 dB
Frequency range	Adjustable
Minimum	100 Mbps
Maximum	12.5 Gbps
Frequency deviation	+500/-5500ppm (+0.05/-0.55%) 30-33 KHz Modulation Rate
Bandwidth deviation	± 2% Measured with 1100 pattern at room temperature over 500 kHz to 12 MHz BW setting. Increased deviation for BW settings below 500 KHz.
Peaking deviation	± 10% of setting or 0.2 dB
Measured edge density deviation	± 1%
Phase error output	Linear Volts/UI of phase error depends on edge density and is not calibrated. Bandwidth limited.
Connector type	SMA
Impedance	50 Ω
Coupling	DC
Frequency Track Output	Volts/PPM of frequency variation (e.g. 5000 PPM gives 5 V _{pp}) is not calibrated.
Connector type	SMA
Impedance	50 Ω
Coupling	DC

Table 4: Characteristics (cont.)

Specifications	Characteristics
Trigger input	External CR lock request
Connector type	SMA
Impedance	50 Ω
Coupling	DC (to 0 volts)
Threshold	1.5 V
Pulse width	50 ns minimum
Trigger output	External lock status indicator
Connector type	SMA
Impedance	50 Ω
Coupling	DC
Latency	300 ms maximum

Table 5: Power consumption, fuses, and cooling

Specifications	Characteristics
Source voltage and frequency	100 VAC to 240 VAC at 50 Hz to 60 Hz
Fuse rating	3.15 A
Power requirements	150 W maximum

Table 6: Mechanical

Specifications	Characteristics
Weight	20 lbs (9.1 kg)
Overall dimensions	15.5 in. W x 3.75 in. H x 13.75 in. D (394 mm W x 95 mm H x 337 mm x D) The dimensions do not include feet or protruding connectors.

Table 7: Environmental specifications

Specification	Characteristics
Dynamics	
Vibration (operating)	Meets MIL-PRF-28800F Class 3
Shock	Meets MIL-PRF-28800F Class 3
Bench handling (operating)	Meets MIL-PRF-28800F Class 3

Table 7: Environmental specifications (cont.)

Specification	Characteristics
Atmospherics	
Temperature	
Operating	+10 °C to +40 °C
Nonoperating	-22 °C to +60 °C
Relative humidity	
Operating	20% to 80% relative humidity with a maximum wet bulb temperature of +29 °C at or below +40 °C.
Nonoperating	5% to 90% relative humidity with a maximum wet bulb temperature of +29 °C at or b below +60 °C.
Altitude	
Operating	3,000 m (9,842 ft.)
Non-operating	12,190 m (40,000 ft.)

Table 8: Electromagnetic specifications

Specification	Characteristic
Emissions	The instrument meets or exceeds the EMC requirements of the following standards: EN61326-1 European Community Requirements
Susceptibility	The instrument meets or exceeds the EMC requirements of the following standards: EN61326-1 European Community Requirements

Certifications

Table 9: Certifications and compliances

Category	Standards or description																		
EC Declaration of Conformity - EMC	<p>Complies with the following requirements of the EMC directive EN61326:</p> <table border="0"> <tr> <td data-bbox="492 531 808 562">EN 61326</td> <td data-bbox="816 531 1458 594">EMC requirements for Class A electrical equipment for measurement, control and laboratory use, Annex D.</td> </tr> <tr> <td data-bbox="492 604 808 636">EN 61000-4-2</td> <td data-bbox="816 604 1458 636">Electrostatic discharge</td> </tr> <tr> <td data-bbox="492 646 808 678">IEC 61000-4-3</td> <td data-bbox="816 646 1458 678">RF electromagnetic field immunity</td> </tr> <tr> <td data-bbox="492 688 808 720">IEC 61000-4-4</td> <td data-bbox="816 688 1458 720">Electrical fast transient / burst immunity</td> </tr> <tr> <td data-bbox="492 730 808 762">IEC 61000-4-5</td> <td data-bbox="816 730 1458 762">Power line surge immunity</td> </tr> <tr> <td data-bbox="492 772 808 804">IEC 61000-4-6</td> <td data-bbox="816 772 1458 804">Conducted RF immunity</td> </tr> <tr> <td data-bbox="492 814 808 846">IEC 61000-4-11</td> <td data-bbox="816 814 1458 846">Voltage dips and interruptions immunity</td> </tr> <tr> <td data-bbox="492 856 808 888">EN 61000-3-2</td> <td data-bbox="816 856 1458 888">AC Power Harmonic Current Emissions</td> </tr> <tr> <td data-bbox="492 898 808 930">EN 61000-3-3</td> <td data-bbox="816 898 1458 930">Voltage changes, fluctuations, and flicker</td> </tr> </table>	EN 61326	EMC requirements for Class A electrical equipment for measurement, control and laboratory use, Annex D.	EN 61000-4-2	Electrostatic discharge	IEC 61000-4-3	RF electromagnetic field immunity	IEC 61000-4-4	Electrical fast transient / burst immunity	IEC 61000-4-5	Power line surge immunity	IEC 61000-4-6	Conducted RF immunity	IEC 61000-4-11	Voltage dips and interruptions immunity	EN 61000-3-2	AC Power Harmonic Current Emissions	EN 61000-3-3	Voltage changes, fluctuations, and flicker
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