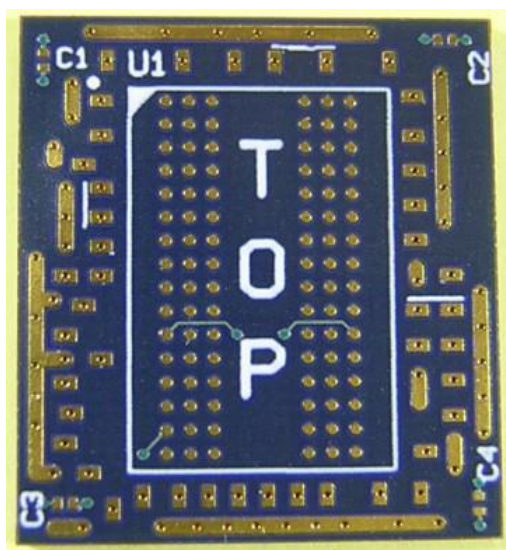
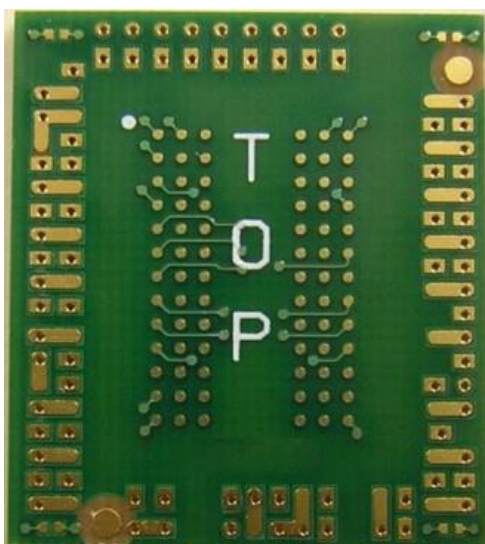


N2114A and N2115A DDR4 BGA Interposers for Infiniium Oscilloscopes

Superior probing for DDR4 compliance test and debug



Introduction

The DDR4 BGA interposers provide signal access to clock, strobe, data, address and command signals of the DDR4 BGA package for making electrical, timing and eye diagram measurements with an Infiniium oscilloscope. The DDR4 JEDEC¹ specification is defined at the DRAM ballout, and the ballout is difficult to access. The BGA interposer provides direct signal access to the BGA package for true compliance testing.

The DDR4 BGA interposers are soldered between the DRAM and PC board or DIMM raw card where the DRAM would normally be soldered. They are designed with the PCB or DIMM footprint on the bottom side and the DRAM footprint on the top side. The BGA interposer passes the signals from the memory controller chip and DRAM directly to the top side of the BGA interposer where they can be accessed with oscilloscope probes.

Buried resistors placed at the signals inside the BGA interposer connect the probed signals to solder pads designed to work with InfiniMax differential or single-ended solder-in probe heads. These resistors isolate the DDR4 signal and the probe loading effect. This design minimizes capacitive loading of the probe heads and allows high-speed operation without impact on signal integrity.

Probing at the right location is also an important consideration for DDR4 measurement. Many designs have vias or designed-in probe points, but they do not always produce good signal integrity. Probing at the wrong location could cause signal reflection, resulting in non-monotonic edges. This will cause error in your tests such as slew rate, setup and hold time measurements.

When used with N6462A/B DDR4 compliance test application, the BGA interposers provide a fast and easy way to test, debug and characterize your DDR4 designs. The tests covered by the N6462A/B software are based on the JEDEC DDR4 SDRAM specification. The test application offers a user-friendly setup wizard and a comprehensive report that includes margin analysis.

¹ The JEDEC (Joint Electronic Device Engineering Council) Solid State Technology Association is a semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronic industry.

Features

- Provides signal access points for DDR4 DRAM x4, x8 and x16 packages using JEDEC-standard common BGA footprints to the oscilloscope
- Buried resistors provide signal isolation and minimize capacitive loading
- Perimeter solder-down test points can be used with Logic Analyzer flying leads or Oscilloscope solder-down probe tips to access signals
- Effective bandwidth may be extended with InfiniiSim Waveform Transformation software
- Measurement timing skews reduced by matched trace lengths from DDR4 balls to test points
- Capacitive decoupling of the power and ground is achieved with plane layers within the stack-up of the interposer and four SMT capacitors
- Probing compatibility with InfiniiMax probe, which includes E2677A, N5381A, and N5425A/N5426A differential solder-in probe heads

Installing the DDR4 BGA interposer

The DDR4 BGA interposer is installed by soldering onto the BGA footprint of the PC board or DIMM card where the DRAM normally would be soldered. Then, solder the DDR4 DRAM to the top side of the BGA interposer. A riser may be soldered below the interposer to provide a lift to avoid interference with the adjacent components on the board or DIMM. These attachment steps may occur in any order.

The probe is designed to tolerate lead-free soldering temperature profiles. However, we recommend you apply the minimum temperature required for soldering and use the minimum number of heating and cooling cycles to reduce risk of any damage to the probe. The probe is supplied with lead-free solder balls.

We recommend you attach the BGA interposer during the manufacturing process. For designs that are manufactured, it will require expertise to attach the BGA interposers. If you lack the in-house expertise to attach the BGA interposer, you may wish to work with a contract manufacturer with this expertise that may be willing to perform the attachment for a fee. You can find more information on BGA soldering and rework techniques that may be useful in attaching the probe at:

<http://www.circuitrework.com/guides/9-1-1.shtml>



Figure 1. Photo of stacked DIMM-Riser-Interposer-DDR.

Installing the InfiniiMax probe

You can use the DDR4 BGA interposer with various InfiniiMax solder-in probes. Instructions that come with the InfiniiMax probe provide details on the proper soldering procedures for the InfiniiMax probe heads.

DDR4 BGA interposer dimensions, pad numbering and location

Model number: N2114A

Ball count: 78

Size: 16 mm x 18 mm

Connectors: Solder-down test points and solder balls

Signals to be probed

- The DDR4 FBGA Interposer provides access to the DDR4 signals highlighted below and passes all power and ground signals between the system and the memory chip.
- Internal power and ground planes are used within the interposer. All VDD and VDDQ signals share a common power plane. All VSS and VSSQ signals share a common ground plane.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---------|----------|--------|---|-----------|-----------|---------|
| VDD | GND | TDQS_c | A | DM_N/DBI | GND | GND |
| VPP | VDD | DQS_c | B | DQ1 | VDD | ZQ |
| VDD | DQ0 | DQS_t | C | VDD | GND | VDD |
| GND | DQ4 | DQ2 | D | DQ3 | DQ5 | GND |
| GND | VDD | DQ6 | E | DQ7 | VDD | GND |
| VDD | C2/ODT1 | ODT | F | CK_t | CK_c | VDD |
| GND | C0/CKE1 | CKE | G | CS_n | C1/CS1_n | RFU |
| VDD | WE_n/A14 | ACT_n | H | CAS_n/A15 | RAS_n/A16 | GND |
| VrefCA | BG0 | A10/AP | J | A12/BC_n | BG1 | VDD |
| GND | BA0 | A4 | K | A3 | BA1 | GND |
| RESET_n | A6 | A0 | L | A1 | A5 | ALERT_n |
| VDD | A8 | A2 | M | A9 | A7 | VPP |
| GND | A11 | PARITY | N | A17 | A13 | VDD |

Figure 2. Highlighted signals are probed (top view).

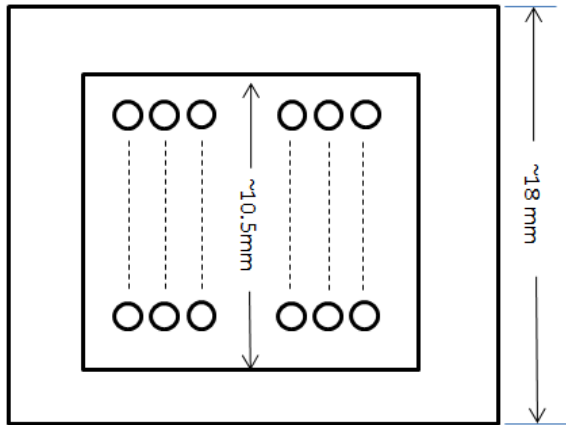
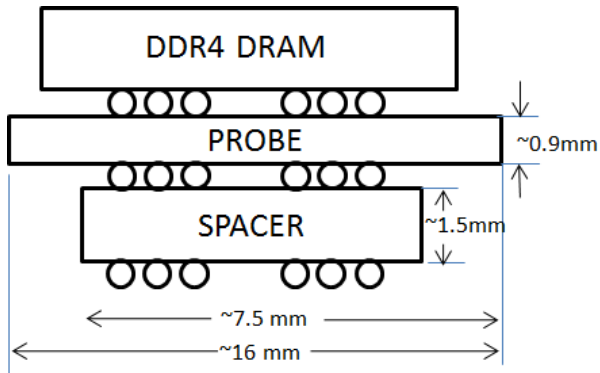


Figure 3. Riser/spacer, Interposer and RAM stack up.

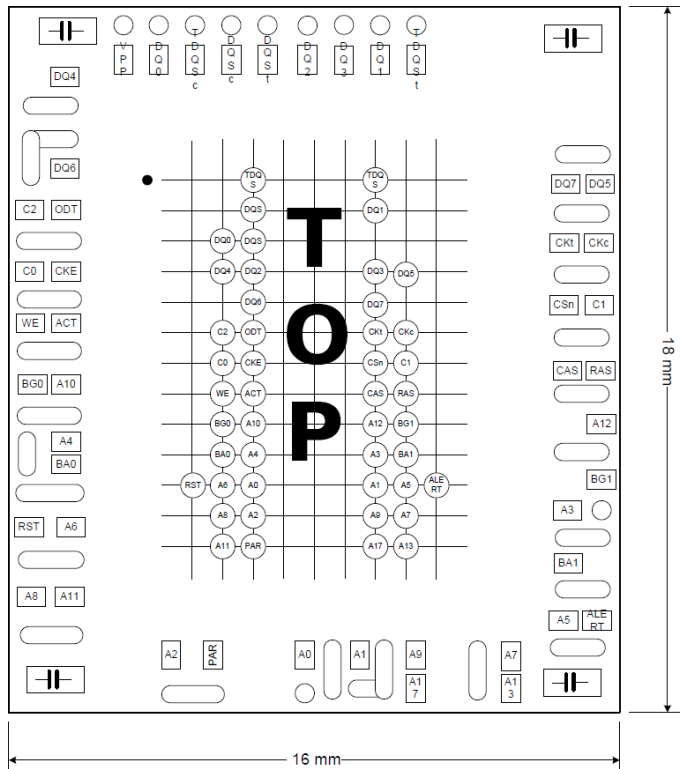


Figure 4. N2114A dimension drawing of interposer.

Model number: N2115A
 Ball count: 96
 Package size: 12.5 mm x 19.0 mm (max)
 Connectors: Solder-down test points and solder balls

Signals to be probed

- The DDR4 FBGA Interposer provides access to the DDR4 signals highlighted below and passes all power and ground signals between the system and the memory chip.
- There is one common power plane in the interposer. The four sets of surface mount (SMT) capacitor pads are connected to that common power plane. The user can probe the power planes using these SMT pads or attach 0201 size SMT filter capacitors to improve power integrity.

| 1 | 2 | 3 | 4 to 6 | 7 | 8 | 9 |
|---------|--------------|--------|--------|-------------|-----------|---------|
| VDDQ | GND | DQU0 | A | DQSU_c | GND | VDDQ |
| VPP | GND | VDD | B | DQSU_t | DQU1 | VDD |
| VDDQ | DQU4 | DQU2 | C | DQU3 | DQU5 | GND |
| VDD | GND | DQU6 | D | DQU7 | GND | VDDQ |
| GND | DMU_n/DBIU_n | GND | E | DML_n/DBI_n | GND | GND |
| GND | VDDQ | DQSL_c | F | DQL1 | VDDQ | ZQ |
| VDDQ | DQL0 | DQSL_t | G | VDD | GND | VDDQ |
| GND | DQL4 | DQL2 | H | DQL3 | DQL5 | GND |
| VDD | VDDQ | DQL6 | J | DQL7 | VDDQ | VDD |
| GND | CKE | ODT | K | CK_t | CK_c | GND |
| VDD | WE_n/ A14 | ACT_n | L | CS_n | RAS_n/A16 | VDD |
| VrefCA | BG0 | A10/AP | M | A12/BC_n | CAS_n/A15 | GND |
| GND | BA0 | A4 | N | A3 | BA1 | TEN |
| RESET_n | A6 | A0 | P | A1 | A5 | ALERT_n |
| VDD | A8 | A2 | R | A9 | A7 | VPP |
| GND | A11 | PARITY | T | NC | A13 | VDD |

Figure 5. Highlighted signals are probed (top view).

Ordering Information

| Model number | Description |
|--------------|---|
| N2114A | x4/8 DDR4 scope optimized BGA interposer with riser. Includes: qty (1) interposer and qty (1) riser |
| N2115A | x16 DDR4 scope optimized BGA interposer with riser. Includes: qty (1) interposer and qty (1) riser |

Note: S parameter for use with InfiniiSim Waveform Transformation Toolset available at

www.keysight.com/find/n2114a and www.keysight.com/find/n2115a.

Recommended oscilloscope and probes

| Data rate | Minimum bandwidth | Minimum channels | Minimum bandwidth |
|-----------------|-------------------|------------------|-----------------------------|
| Up to 3200 MT/s | 13 GHz | 3 | Infinium 90000 and Z-Series |

Probe accessories amplifiers

| Option | Description |
|--------|--------------------------------------|
| 1169A | InfiniiMax II 12-GHz probe amplifier |

InfiniiMax I/II probe heads and accessories

(Compatible with 9000 and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series)

| Option | Description |
|--------|--|
| N5381A | InfiniiMax II 12-GHz differential solder-in probe head and accessories |
| N5382A | InfiniiMax II 12-GHz differential browser |
| E2677A | InfiniiMax II 12-GHz differential solder-in probe head and accessories |
| N5425A | InfiniiMax II 12-GHz ZIF probe head |
| N5426A | InfiniiMax II ZIF tips (x10) |

Related Literature

| Publication title | Publication number |
|---|--------------------|
| E2688A, N5384A High-Speed Serial Data Analysis and Clock Recovery Software for Infiniium Oscilloscopes - Data Sheet | 5989-0108EN |
| EZJIT Plus Jitter Analysis Software for Infiniium Oscilloscopes - Data Sheet | 5989-0109EN |
| Infiniium 90000 Series Oscilloscopes - Data Sheet | 5989-7819EN |
| N5465A InfiniiSim Waveform Transformation Toolset for Infiniium Oscilloscopes - Data Sheet | 5990-4059EN |
| Infiniium 90000 X-Series Oscilloscopes - Data Sheet | 5990-5271EN |

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