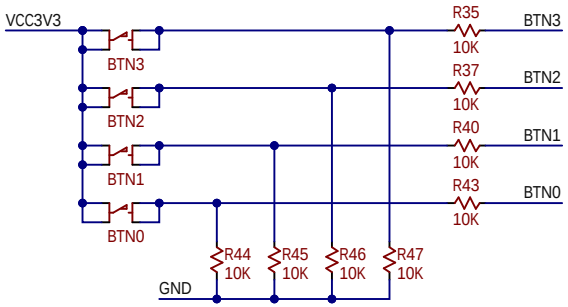
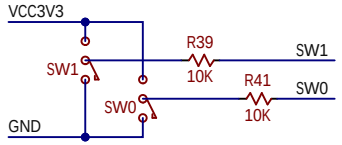






Foot F1

Foot F2

Foot F3

Foot F4

UKCA

PYNQ | Digilent Inc. | Xilinx | Texas Instruments | CE | ROHS | Chinese ROHS

Title	Rev
PYNQ-Z1	F.0

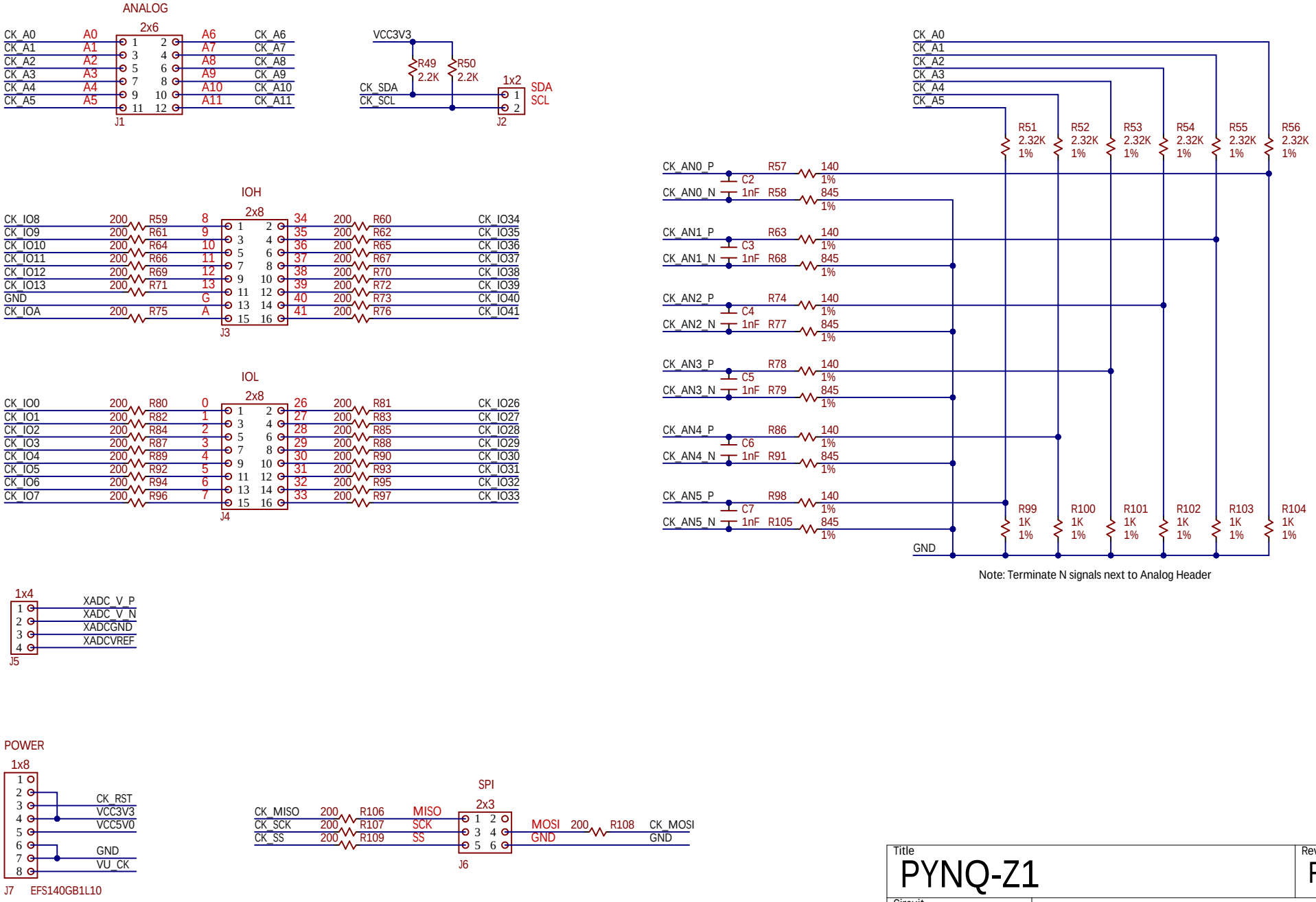
Circuit	PMODs, User I/O
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	1 out of 13

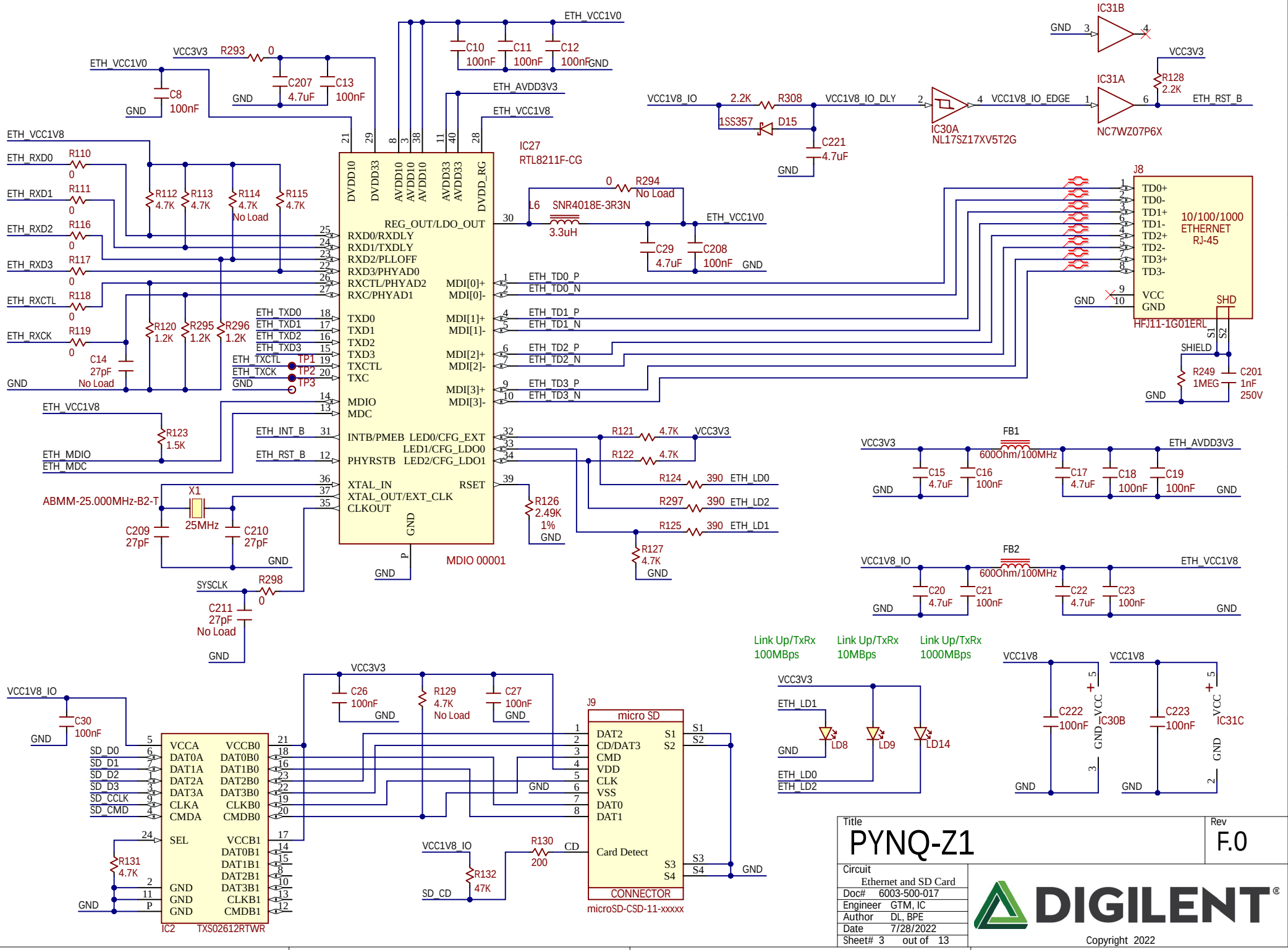
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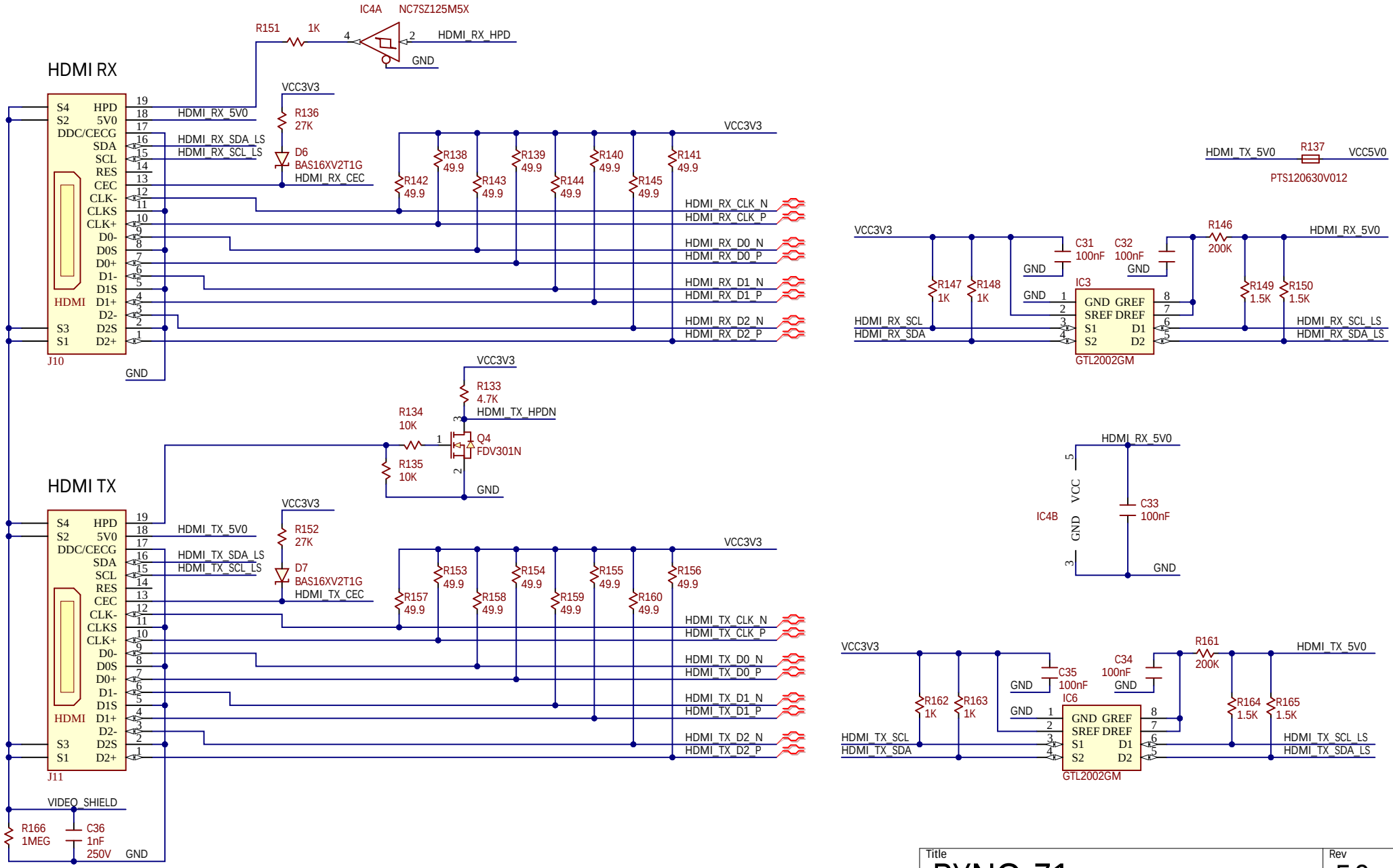
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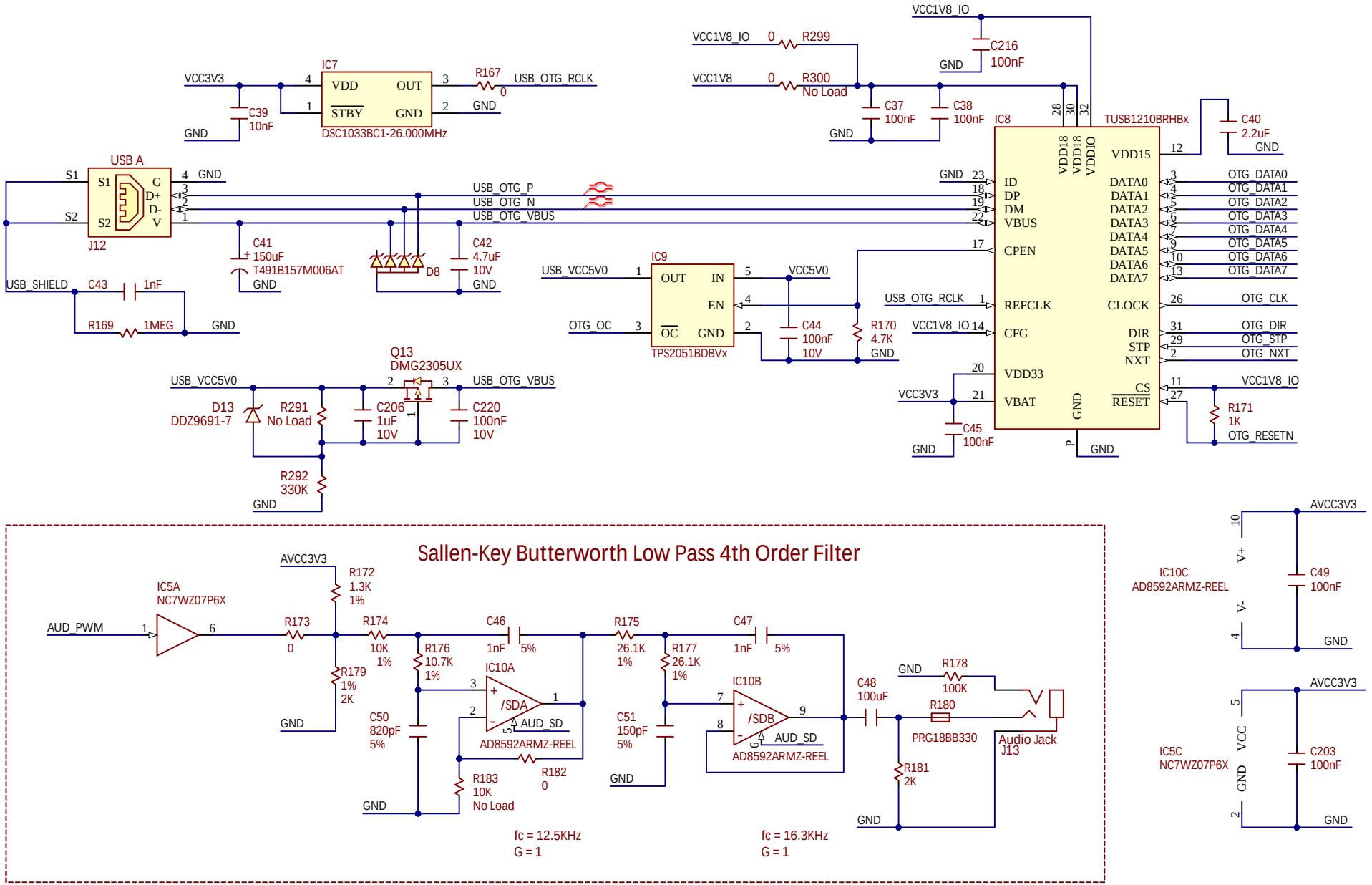

ANALOG
2x6
CK_A0 A0 A6 CK_A6
CK_A1 A1 A7 CK_A7
CK_A2 A2 A8 CK_A8
CK_A3 A3 A9 CK_A9
CK_A4 A4 A10 CK_A10
CK_A5 A5 A11 CK_A11
J1
VCC3V3
R49 2.2K
R50 2.2K
CK_SDA
CK_SCL
1x2
SDA
SCL
J2
IOH
2x8
CK_IO8 200 R59 8 34 200 R60 CK_IO34
CK_IO9 200 R61 9 35 200 R62 CK_IO35
CK_IO10 200 R64 10 36 200 R65 CK_IO36
CK_IO11 200 R66 11 37 200 R67 CK_IO37
CK_IO12 200 R69 12 38 200 R70 CK_IO38
CK_IO13 200 R71 13 39 200 R72 CK_IO39
GND G 40 200 R73 CK_IO40
CK_IOA 200 R75 A 41 200 R76 CK_IO41
J3
IOL
2x8
CK_IO0 200 R80 0 26 200 R81 CK_IO26
CK_IO1 200 R82 1 27 200 R83 CK_IO27
CK_IO2 200 R84 2 28 200 R85 CK_IO28
CK_IO3 200 R87 3 29 200 R88 CK_IO29
CK_IO4 200 R89 4 30 200 R90 CK_IO30
CK_IO5 200 R92 5 31 200 R93 CK_IO31
CK_IO6 200 R94 6 32 200 R95 CK_IO32
CK_IO7 200 R96 7 33 200 R97 CK_IO33
J4
CK_A0
CK_A1
CK_A2
CK_A3
CK_A4
CK_A5
R51 2.32K 1%
R52 2.32K 1%
R53 2.32K 1%
R54 2.32K 1%
R55 2.32K 1%
R56 2.32K 1%
CK_AN0_P R57 140 1%
C2 1nF
CK_AN0_N R58 845 1%
CK_AN1_P R63 140 1%
C3 1nF
CK_AN1_N R68 845 1%
CK_AN2_P R74 140 1%
C4 1nF
CK_AN2_N R77 845 1%
CK_AN3_P R78 140 1%
C5 1nF
CK_AN3_N R79 845 1%
CK_AN4_P R86 140 1%
C6 1nF
CK_AN4_N R91 845 1%
CK_AN5_P R98 140 1%
C7 1nF
CK_AN5_N R105 845 1%
GND
R99 1K 1%
R100 1K 1%
R101 1K 1%
R102 1K 1%
R103 1K 1%
R104 1K 1%
Note: Terminate N signals next to Analog Header
1x4
XADC_V_P
XADC_V_N
XADCGND
XADCVREF
J5
POWER
1x8
CK_RST
VCC3V3
VCC5V0
GND
VU_CK
J7 EFS140GB1L10
SPI
2x3
CK_MISO 200 R106 MISO
CK_SCK 200 R107 SCK
CK_SS 200 R109 SS
MOSI 200 R108 CK_MOSI
GND GND
J6
Title
PYNQ-Z1
Rev
F.0
Circuit
chipKIT IO
Doc# 6003-500-017
Engineer GTM, IC
Author DL, BPE
Date 7/28/2022
Sheet# 2 out of 13
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IC27
RTL8211F-CG
MDIO 00001
IC31B
IC31A
IC30A
NL17SZ17XV5T2G
NC7WZ07P6X
J8
10/100/1000
ETHERNET
RJ-45
HFJ11-1G01ERL
J9
micro SD
CONNECTOR
microSD-CSD-11-xxxxx
IC2
TXS02612RTWR
IC30B
IC31C
FB1
FB2
600Ohm/100MHz
ABMM-25.000MHz-B2-T
25MHz
Link Up/TxRx
100MBps
Link Up/TxRx
10MBps
Link Up/TxRx
1000MBps
Title
PYNQ-Z1
Rev
F.0
Circuit
Ethernet and SD Card
Doc# 6003-500-017
Engineer GTM, IC
Author DL, BPE
Date 7/28/2022
Sheet# 3 out of 13
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Title	PYNQ-Z1
Rev	F.0
Circuit	HDMI
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	4 out of 13

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Title	PYNQ-Z1
Rev	F.0
Circuit	USB HOST, MIC, Audio Out
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	5 out of 13

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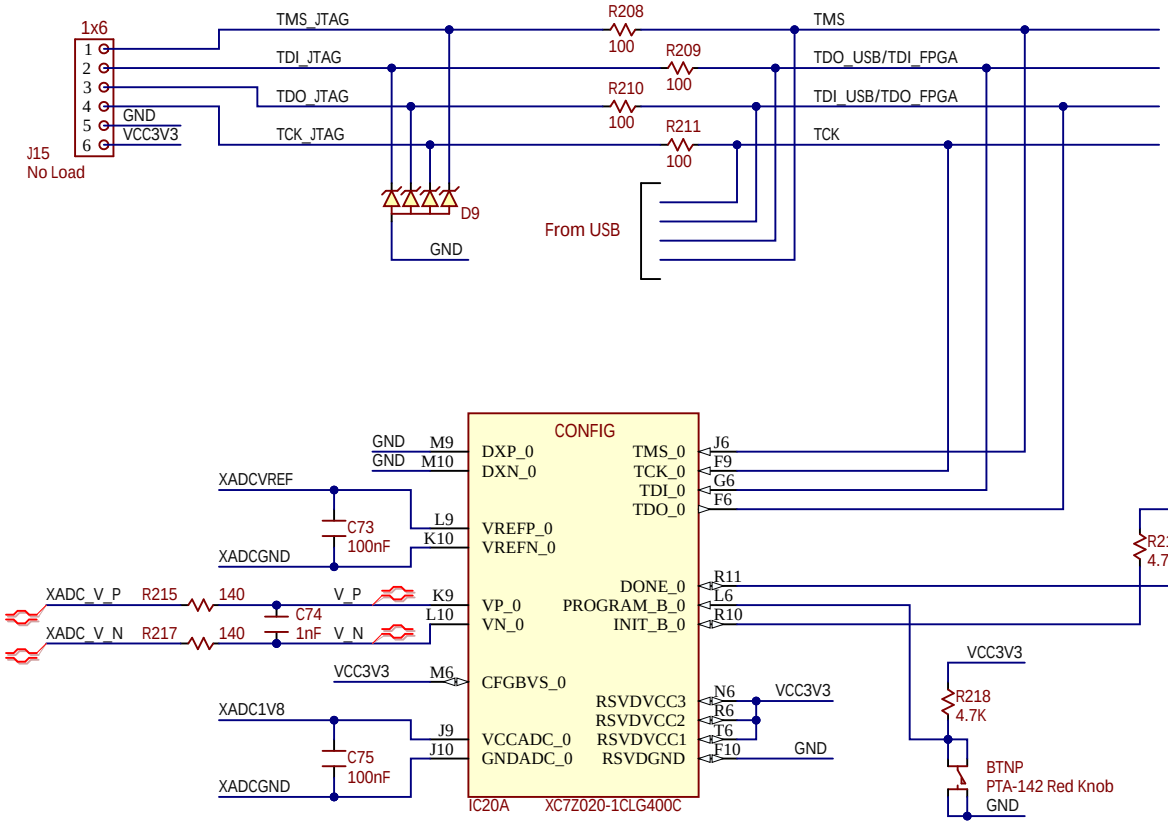
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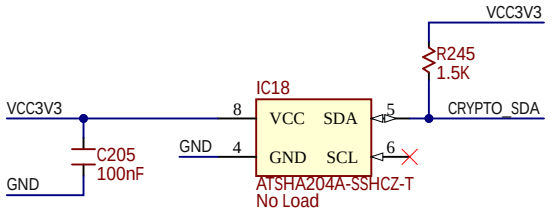
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Title	PYNQ-Z1
Rev	F.0
Circuit	USB PROG, UART
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	6 out of 13

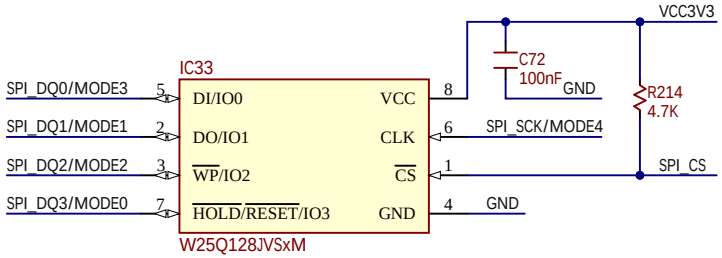
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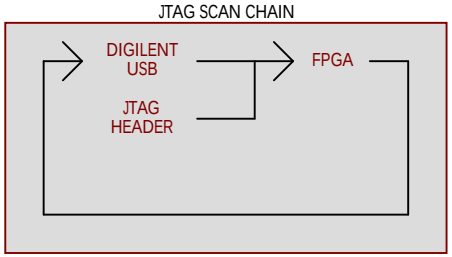
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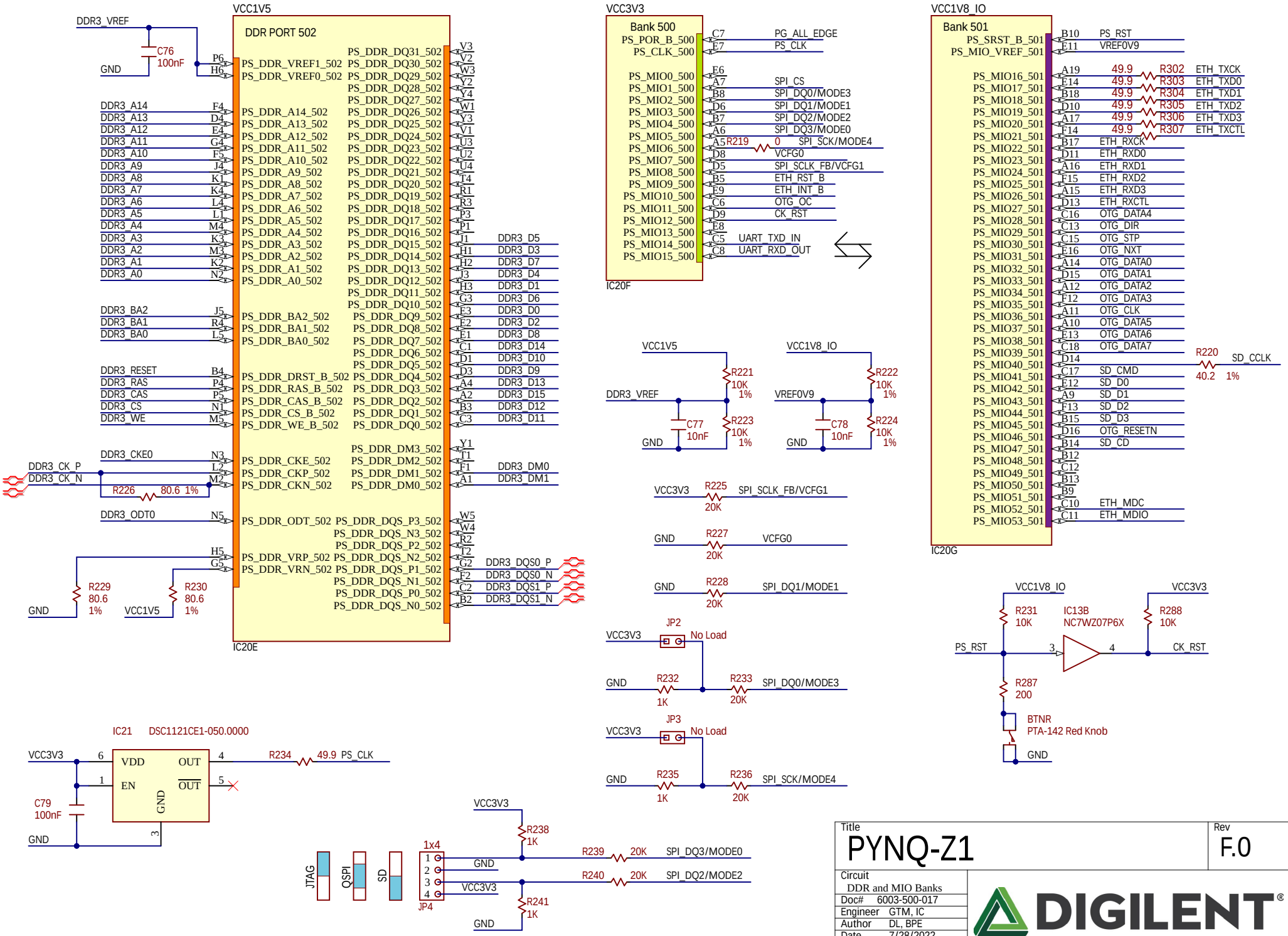
IC33: W25Q128JVSxM (SOIC8) and W25Q128JVPxM (WSON8, 6x5mm) part numbers can be used alternatively, as the PCB footprint works for both.

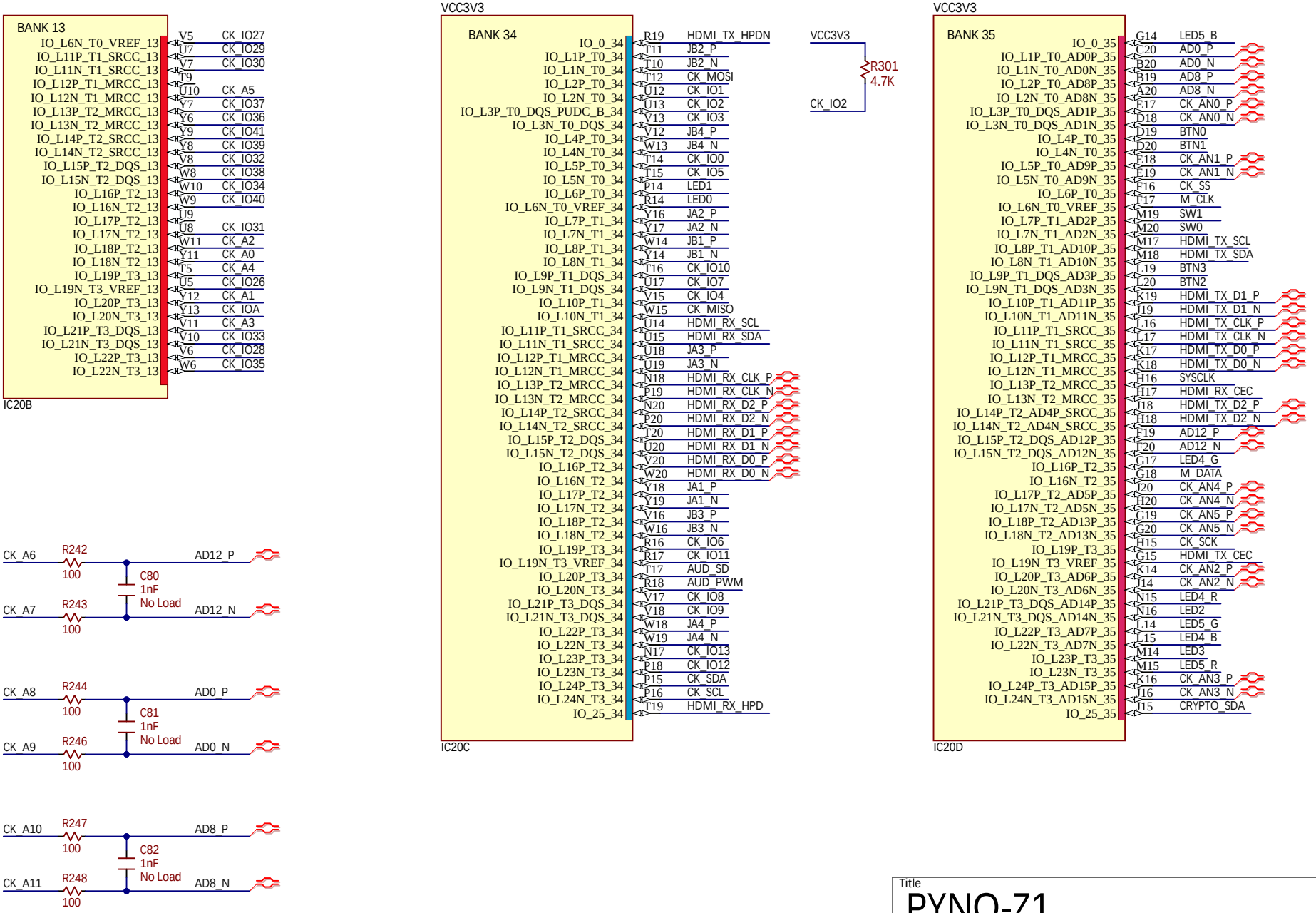




Title	PYNQ-Z1
Rev	F.0
Circuit	FPGA Configuration, Flash
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	7 out of 13

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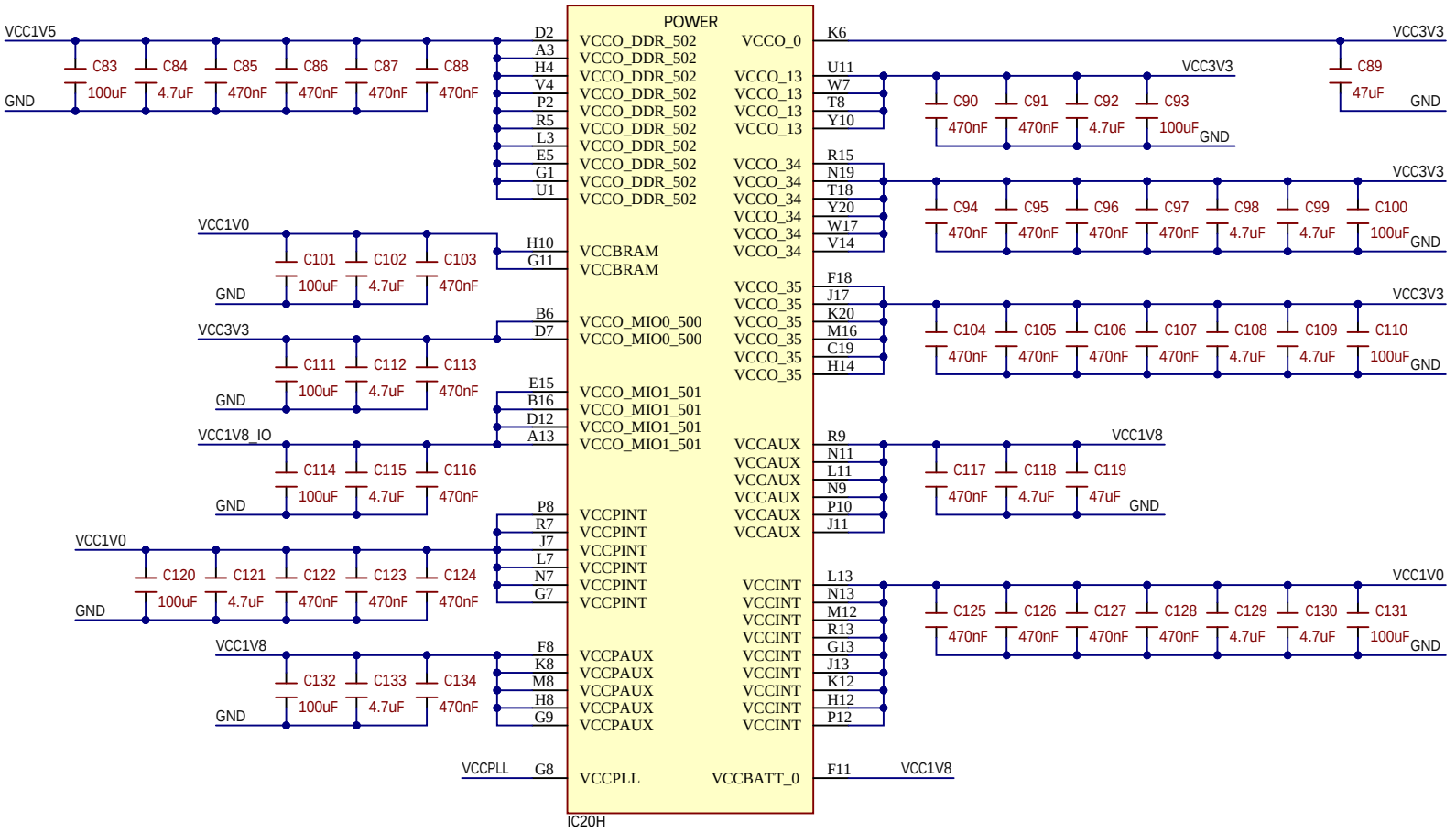

VCC1V5
DDR PORT 502
DDR3_VREF
C76
100nF
GND
PS_DDR_VREF1_502
PS_DDR_VREF0_502
DDR3_A14
DDR3_A13
DDR3_A12
DDR3_A11
DDR3_A10
DDR3_A9
DDR3_A8
DDR3_A7
DDR3_A6
DDR3_A5
DDR3_A4
DDR3_A3
DDR3_A2
DDR3_A1
DDR3_A0
PS_DDR_A14_502
PS_DDR_A13_502
PS_DDR_A12_502
PS_DDR_A11_502
PS_DDR_A10_502
PS_DDR_A9_502
PS_DDR_A8_502
PS_DDR_A7_502
PS_DDR_A6_502
PS_DDR_A5_502
PS_DDR_A4_502
PS_DDR_A3_502
PS_DDR_A2_502
PS_DDR_A1_502
PS_DDR_A0_502
DDR3_BA2
DDR3_BA1
DDR3_BA0
PS_DDR_BA2_502
PS_DDR_BA1_502
PS_DDR_BA0_502
DDR3_RESET
DDR3_RAS
DDR3_CAS
DDR3_CS
DDR3_WE
PS_DDR_DRST_B_502
PS_DDR_RAS_B_502
PS_DDR_CAS_B_502
PS_DDR_CS_B_502
PS_DDR_WE_B_502
DDR3_CKE0
PS_DDR_CKE_502
PS_DDR_CKP_502
PS_DDR_CKN_502
DDR3_CK_P
DDR3_CK_N
R226
80.6 1%
DDR3_ODT0
PS_DDR_ODT_502
PS_DDR_VRP_502
PS_DDR_VRN_502
R229
80.6
1%
R230
80.6
1%
VCC1V5
PS_DDR_DQ31_502
PS_DDR_DQ30_502
PS_DDR_DQ29_502
PS_DDR_DQ28_502
PS_DDR_DQ27_502
PS_DDR_DQ26_502
PS_DDR_DQ25_502
PS_DDR_DQ24_502
PS_DDR_DQ23_502
PS_DDR_DQ22_502
PS_DDR_DQ21_502
PS_DDR_DQ20_502
PS_DDR_DQ19_502
PS_DDR_DQ18_502
PS_DDR_DQ17_502
PS_DDR_DQ16_502
PS_DDR_DQ15_502
PS_DDR_DQ14_502
PS_DDR_DQ13_502
PS_DDR_DQ12_502
PS_DDR_DQ11_502
PS_DDR_DQ10_502
PS_DDR_DQ9_502
PS_DDR_DQ8_502
PS_DDR_DQ7_502
PS_DDR_DQ6_502
PS_DDR_DQ5_502
PS_DDR_DQ4_502
PS_DDR_DQ3_502
PS_DDR_DQ2_502
PS_DDR_DQ1_502
PS_DDR_DQ0_502
PS_DDR_DM3_502
PS_DDR_DM2_502
PS_DDR_DM1_502
PS_DDR_DM0_502
PS_DDR_DQS_P3_502
PS_DDR_DQS_N3_502
PS_DDR_DQS_P2_502
PS_DDR_DQS_N2_502
PS_DDR_DQS_P1_502
PS_DDR_DQS_N1_502
PS_DDR_DQS_P0_502
PS_DDR_DQS_N0_502
DDR3_D5
DDR3_D3
DDR3_D7
DDR3_D4
DDR3_D1
DDR3_D6
DDR3_D0
DDR3_D2
DDR3_D8
DDR3_D14
DDR3_D10
DDR3_D9
DDR3_D13
DDR3_D15
DDR3_D12
DDR3_D11
DDR3_DM0
DDR3_DM1
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DQS1_P
DDR3_DQS1_N
IC20E
VCC3V3
Bank 500
PS_POR_B_500
PS_CLK_500
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
PG_ALL_EDGE
PS_CLK
SPI_CS
SPI_DQ0/MODE3
SPI_DQ1/MODE1
SPI_DQ2/MODE2
SPI_DQ3/MODE0
R219
0
SPI_SCK/MODE4
VCFG0
SPI_SCLK_FB/VCFG1
ETH_RST_B
ETH_INT_B
OTG_OC
CK_RST
UART_TXD_IN
UART_RXD_OUT
IC20F
VCC1V8_IO
Bank 501
PS_SRST_B_501
PS_MIO_VREF_501
PS_MIO16_501
PS_MIO17_501
PS_MIO18_501
PS_MIO19_501
PS_MIO20_501
PS_MIO21_501
PS_MIO22_501
PS_MIO23_501
PS_MIO24_501
PS_MIO25_501
PS_MIO26_501
PS_MIO27_501
PS_MIO28_501
PS_MIO29_501
PS_MIO30_501
PS_MIO31_501
PS_MIO32_501
PS_MIO33_501
PS_MIO34_501
PS_MIO35_501
PS_MIO36_501
PS_MIO37_501
PS_MIO38_501
PS_MIO39_501
PS_MIO40_501
PS_MIO41_501
PS_MIO42_501
PS_MIO43_501
PS_MIO44_501
PS_MIO45_501
PS_MIO46_501
PS_MIO47_501
PS_MIO48_501
PS_MIO49_501
PS_MIO50_501
PS_MIO51_501
PS_MIO52_501
PS_MIO53_501
PS_RST
VREF0V9
R302 49.9 ETH_TXCK
R303 49.9 ETH_TXD0
R304 49.9 ETH_TXD1
R305 49.9 ETH_TXD2
R306 49.9 ETH_TXD3
R307 49.9 ETH_TXCTL
ETH_RXCK
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXCTL
OTG_DATA4
OTG_DIR
OTG_STP
OTG_NXT
OTG_DATA0
OTG_DATA1
OTG_DATA2
OTG_DATA3
OTG_CLK
OTG_DATA5
OTG_DATA6
OTG_DATA7
R220
40.2 1%
SD_CCLK
SD_CMD
SD_D0
SD_D1
SD_D2
SD_D3
OTG_RESETN
SD_CD
ETH_MDC
ETH_MDIO
IC20G
VCC1V5
R221
10K
1%
DDR3_VREF
C77
10nF
GND
R223
10K
1%
VCC1V8_IO
R222
10K
1%
VREF0V9
C78
10nF
GND
R224
10K
1%
VCC3V3
R225
20K
SPI_SCLK_FB/VCFG1
GND
R227
20K
VCFG0
GND
R228
20K
SPI_DQ1/MODE1
JP2
No Load
VCC3V3
GND
R232
1K
R233
20K
SPI_DQ0/MODE3
JP3
No Load
VCC3V3
GND
R235
1K
R236
20K
SPI_SCK/MODE4
VCC1V8_IO
R231
10K
IC13B
NC7WZ07P6X
R288
10K
VCC3V3
PS_RST
3
4
CK_RST
R287
200
BTNR
PTA-142 Red Knob
GND
IC21
DSC1121CE1-050.0000
VCC3V3
6
VDD
OUT
4
R234
49.9 PS_CLK
1
EN
GND
OUT
5
C79
100nF
GND
3
JTAG
QSPI
SD
1x4
1
2
3
4
JP4
VCC3V3
R238
1K
R239
20K
SPI_DQ3/MODE0
GND
R240
20K
SPI_DQ2/MODE2
VCC3V3
R241
1K
GND
Title
PYNQ-Z1
Rev
F.0
Circuit
DDR and MIO Banks
Doc# 6003-500-017
Engineer GTM, IC
Author DL, BPE
Date 7/28/2022
Sheet# 8 out of 13
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Title	PYNQ-Z1
Rev	F.0
Circuit	FPGA Banks, Anti Alias Filt.
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	9 out of 13

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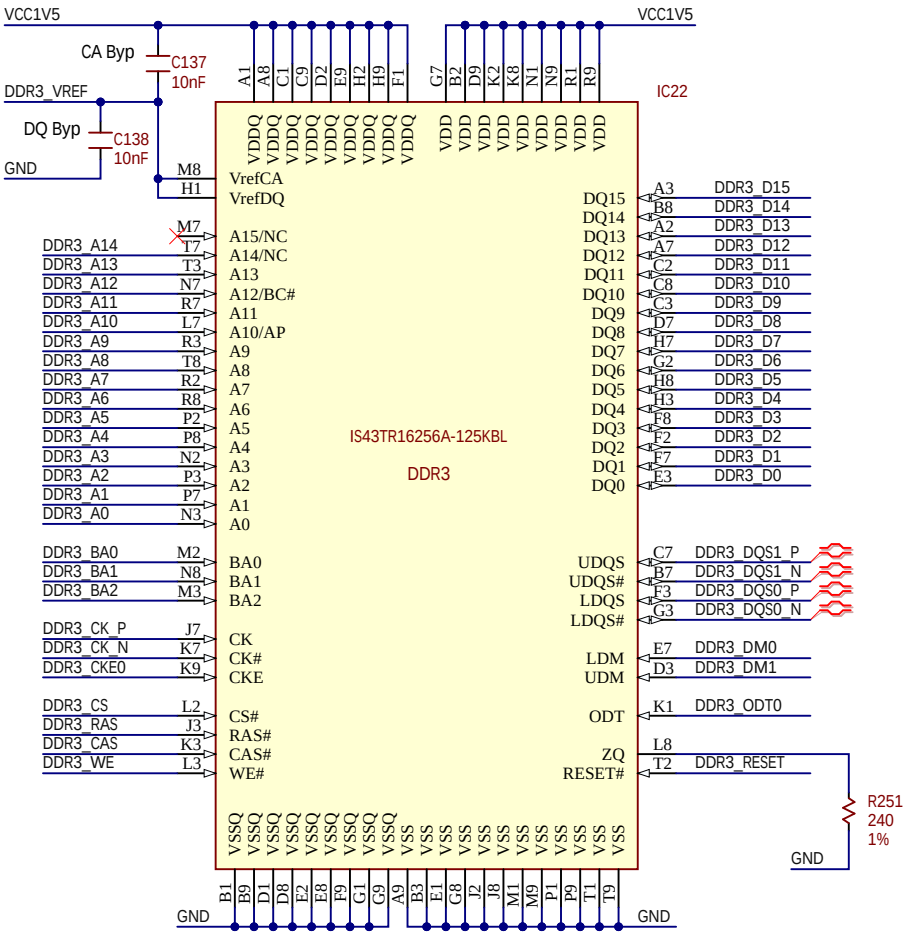
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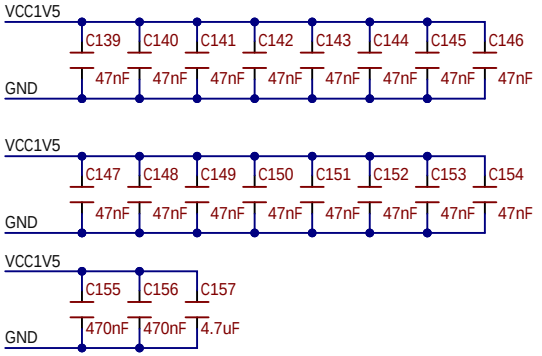


Title	PYNQ-Z1
Rev	F.0
Circuit	FPGA Power
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	10 out of 13

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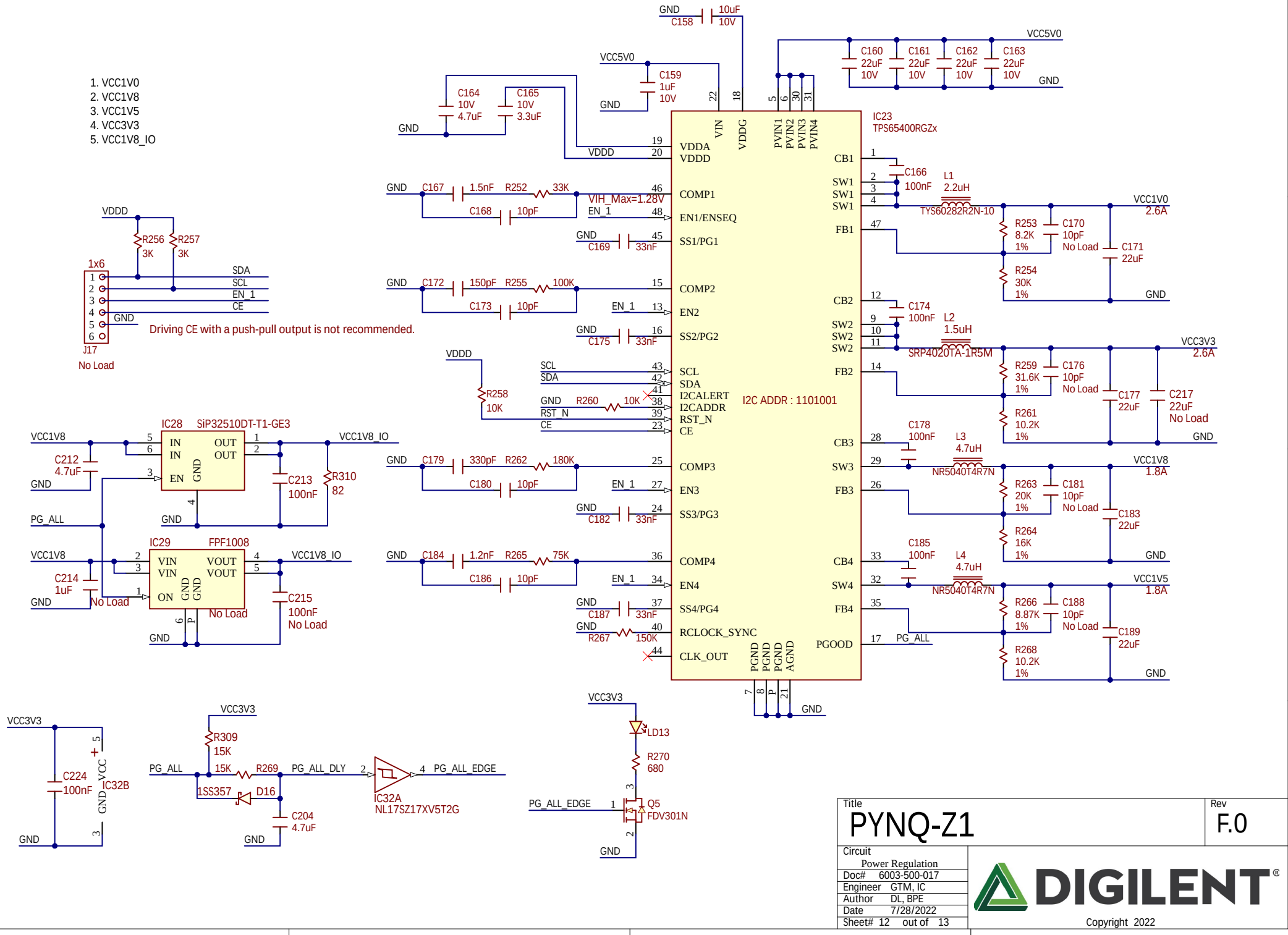






Title	PYNQ-Z1
Rev	F.0
Circuit	DDR3 Memory
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	11 out of 13

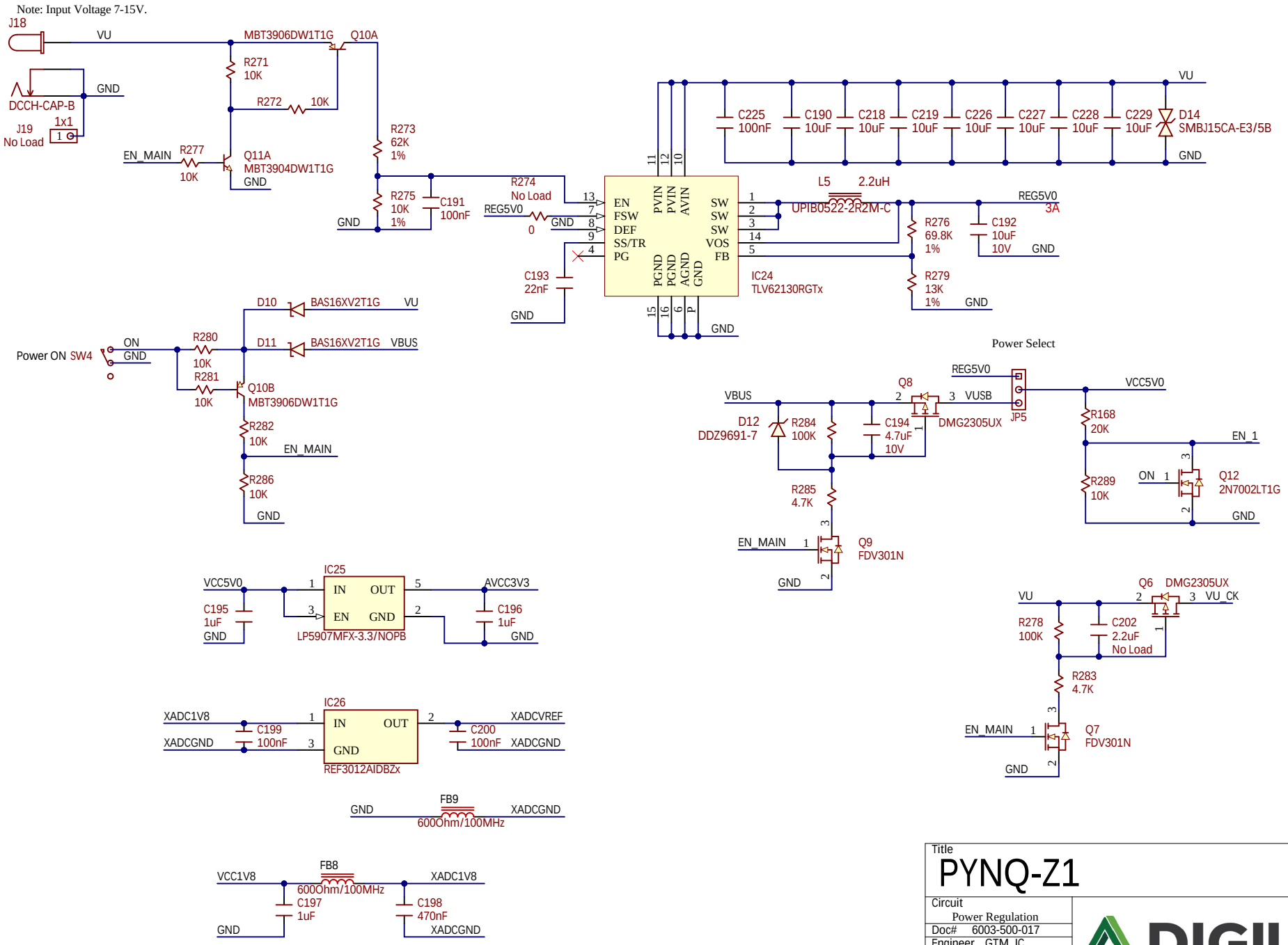
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Title	PYNQ-Z1
Rev	F.0
Circuit	Power Regulation
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
Sheet#	12 out of 13

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Note: Input Voltage 7-15V.



Title	PYNQ-Z1
Rev	F.0
Circuit	Power Regulation
Doc#	6003-500-017
Engineer	GTM, IC
Author	DL, BPE
Date	7/28/2022
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