Genesys ZU

Variant: 3EG

11/13/2019

Rev B.1

Title	Genesys ZU-3EG
Rev	B.1
Circuit	
Doc#	500-383
Engineer	EG
Author	IC
Date	11/13/2019
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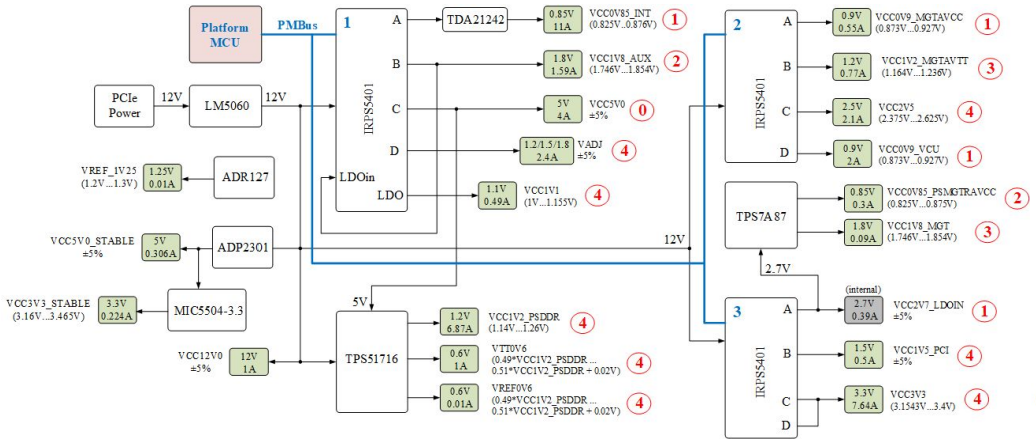
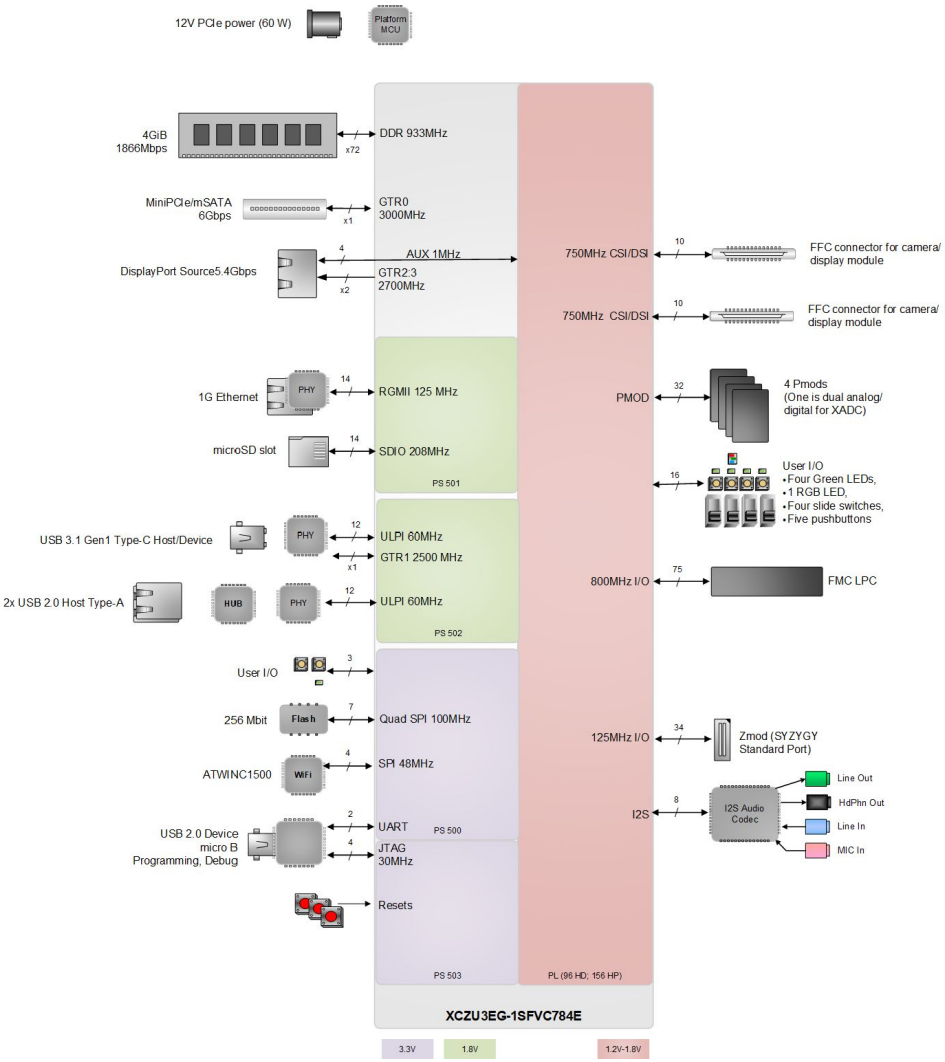
Power Tree



Block Diagram



SHIELD F Foot F1 | SHIELD F Foot F2 | SHIELD F Foot F3 | Foot F4

Foot F5 | SHIELD F Foot F6 | SHIELD F Foot F7 | Foot F8

No Load F9 | No Load F10

Genesys ZU | Insert Contacts Down

Chinese ROHS | ROHS | Digilent Inc. | CE | Xilinx

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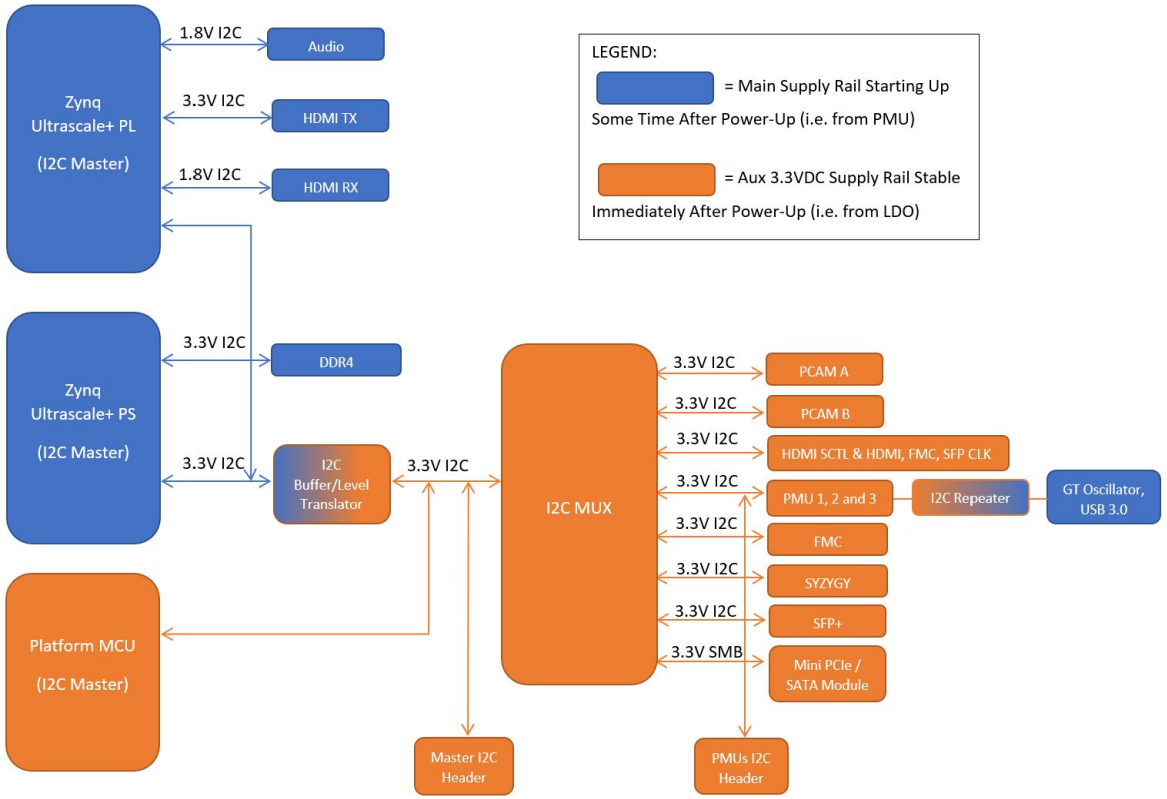
I2C Diagram



Title	Genesys ZU-3EG
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Circuit	I2C Diagram
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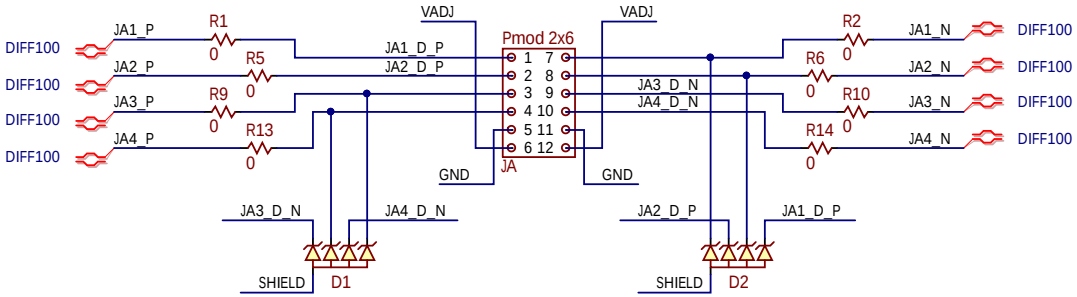
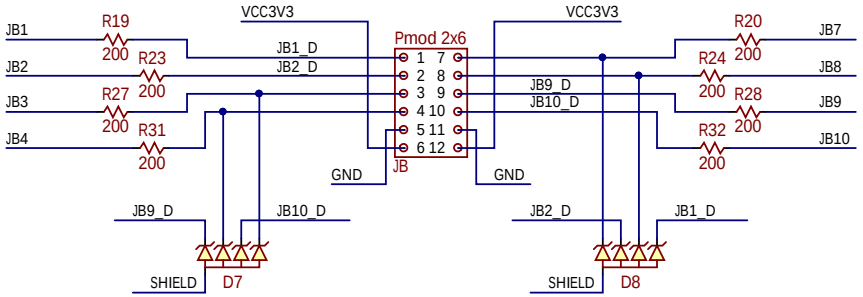
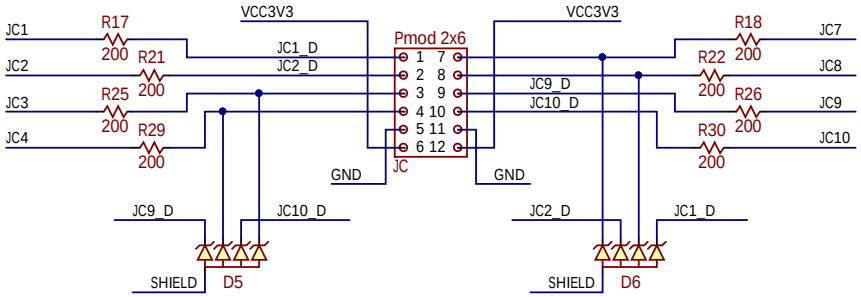
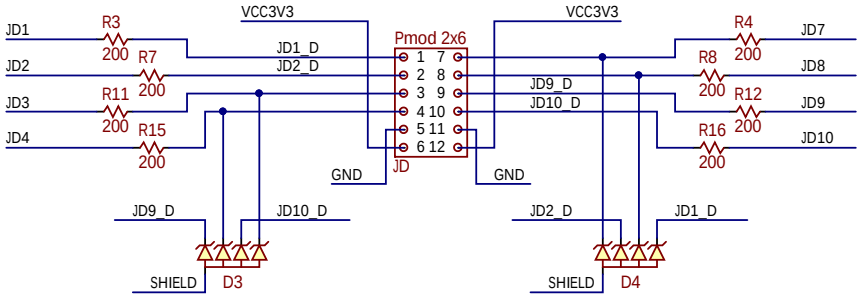
XADC PMOD

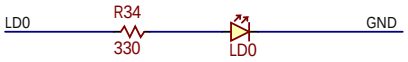




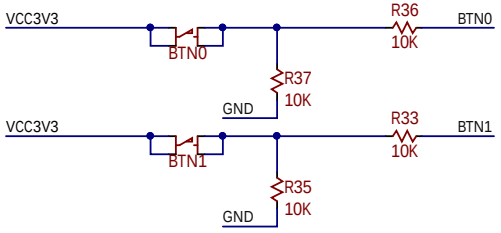




MIO LED



MIO BUTTONS



Title	Genesys ZU-3EG
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Copyright	2019
Circuit	PMODs, MIO BUTTON
Doc#	500-383
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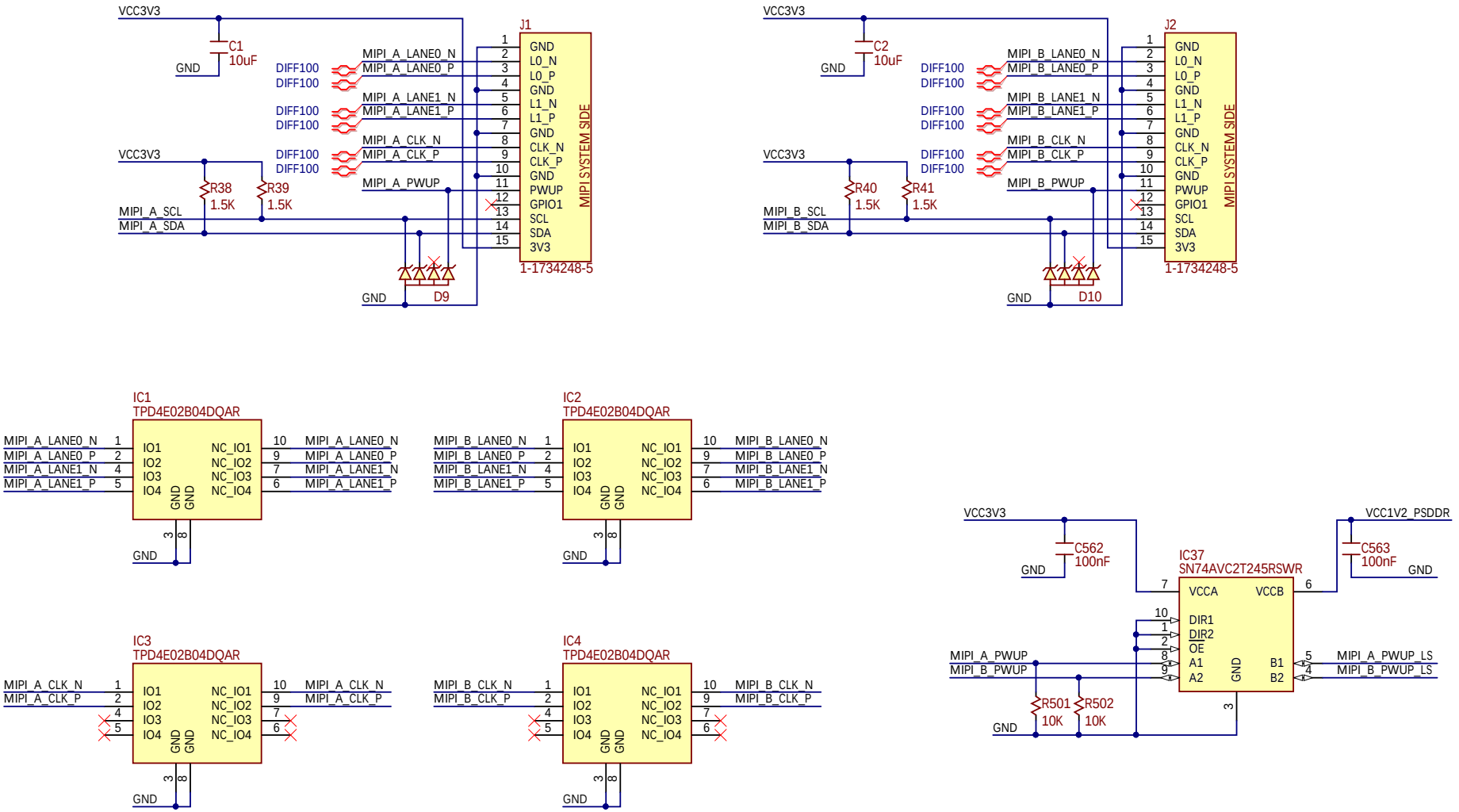

Title	Genesys ZU-3EG
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Copyright	2019
Circuit	MIPI Interfaces
Doc#	500-383
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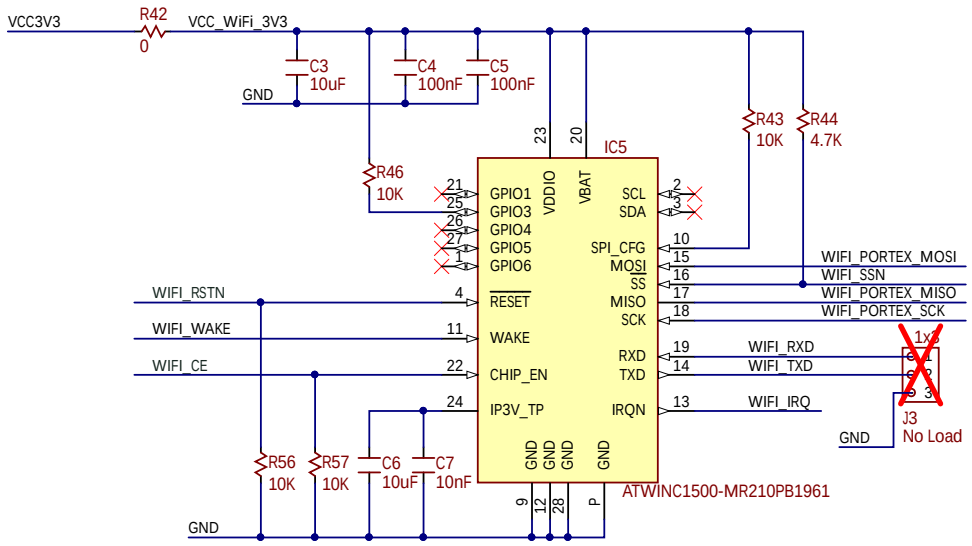
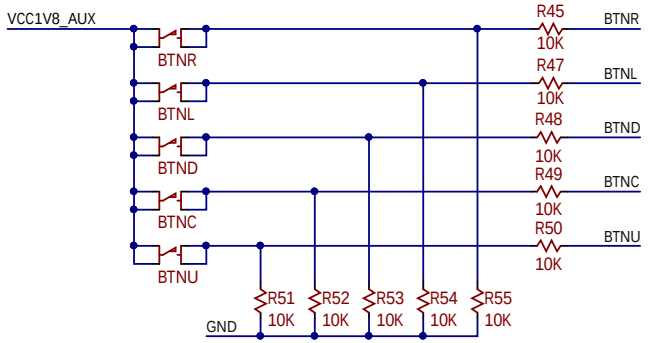
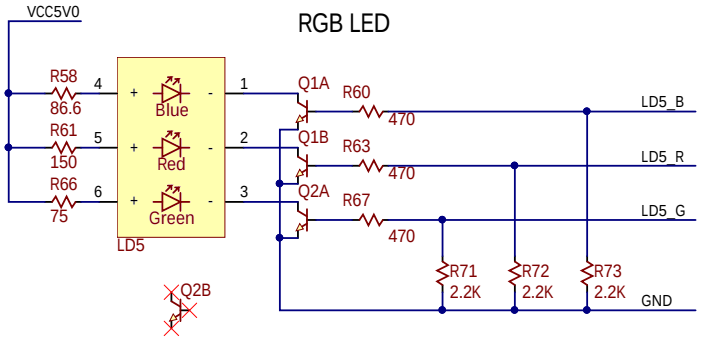


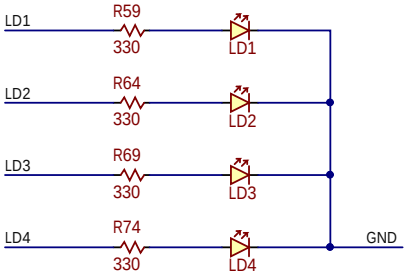
PL BUTTONS



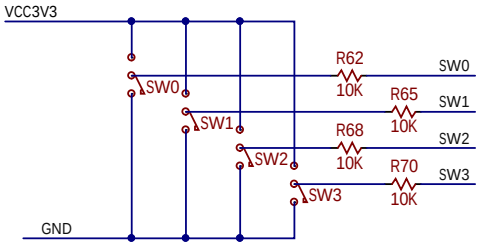
RGB LED



PL LEDS



PL SWITCHES



Title	Genesys ZU-3EG
Rev	B.1
Copyright	2019
Circuit	WI-FI, LEDs, BUTTONS etc.
Doc#	500-383
Engineer	EG
Author	IC
Date	11/13/2019
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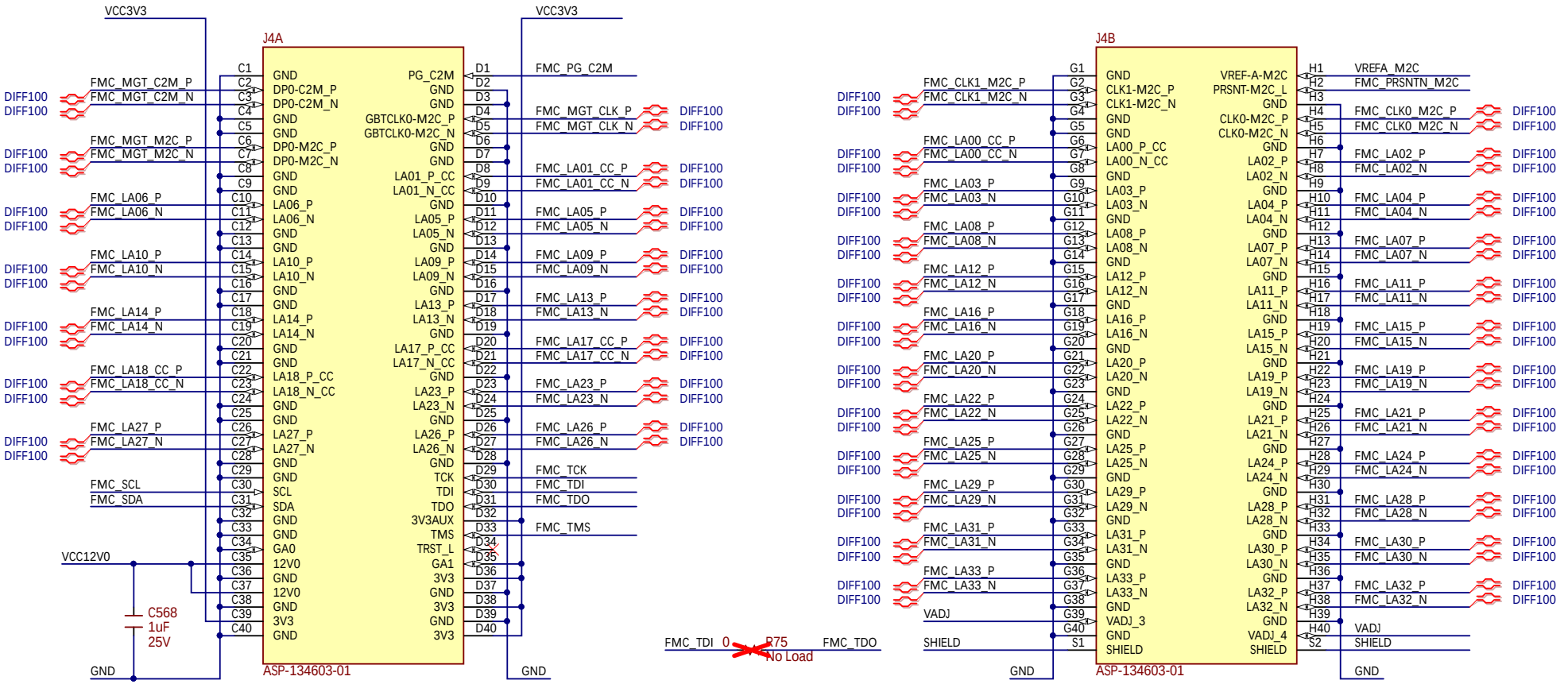

Title	Genesys ZU-3EG
Rev	B.1
Copyright	2019
Circuit	FMC LPC
Doc#	500-383
Engineer	EG
Author	IC
Date	11/13/2019
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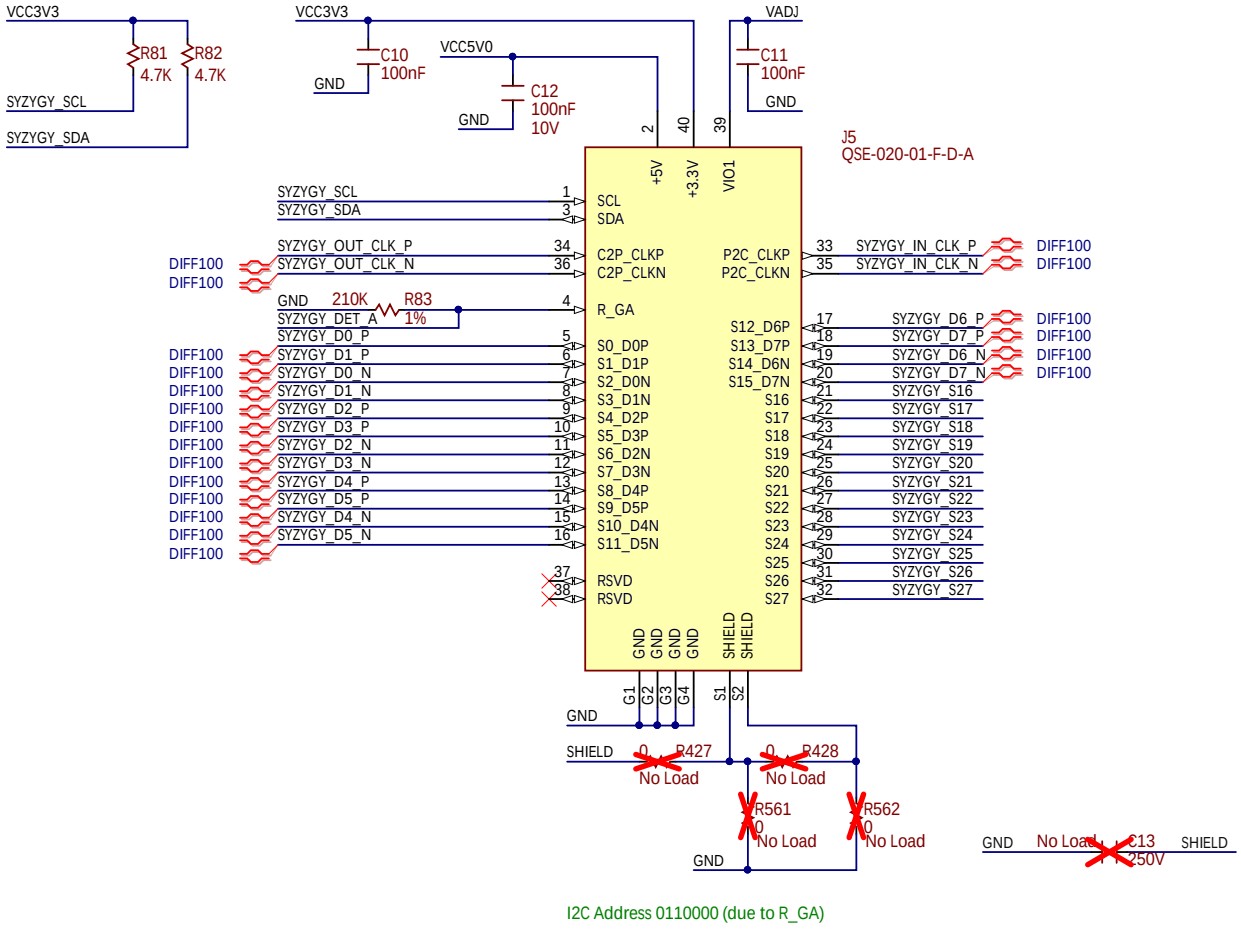

Title	Genesys ZU-3EG
Rev	B.1
Copyright	2019
Circuit	SYZYGY Standard Port
Doc#	500-383
Engineer	EG
Author	IC
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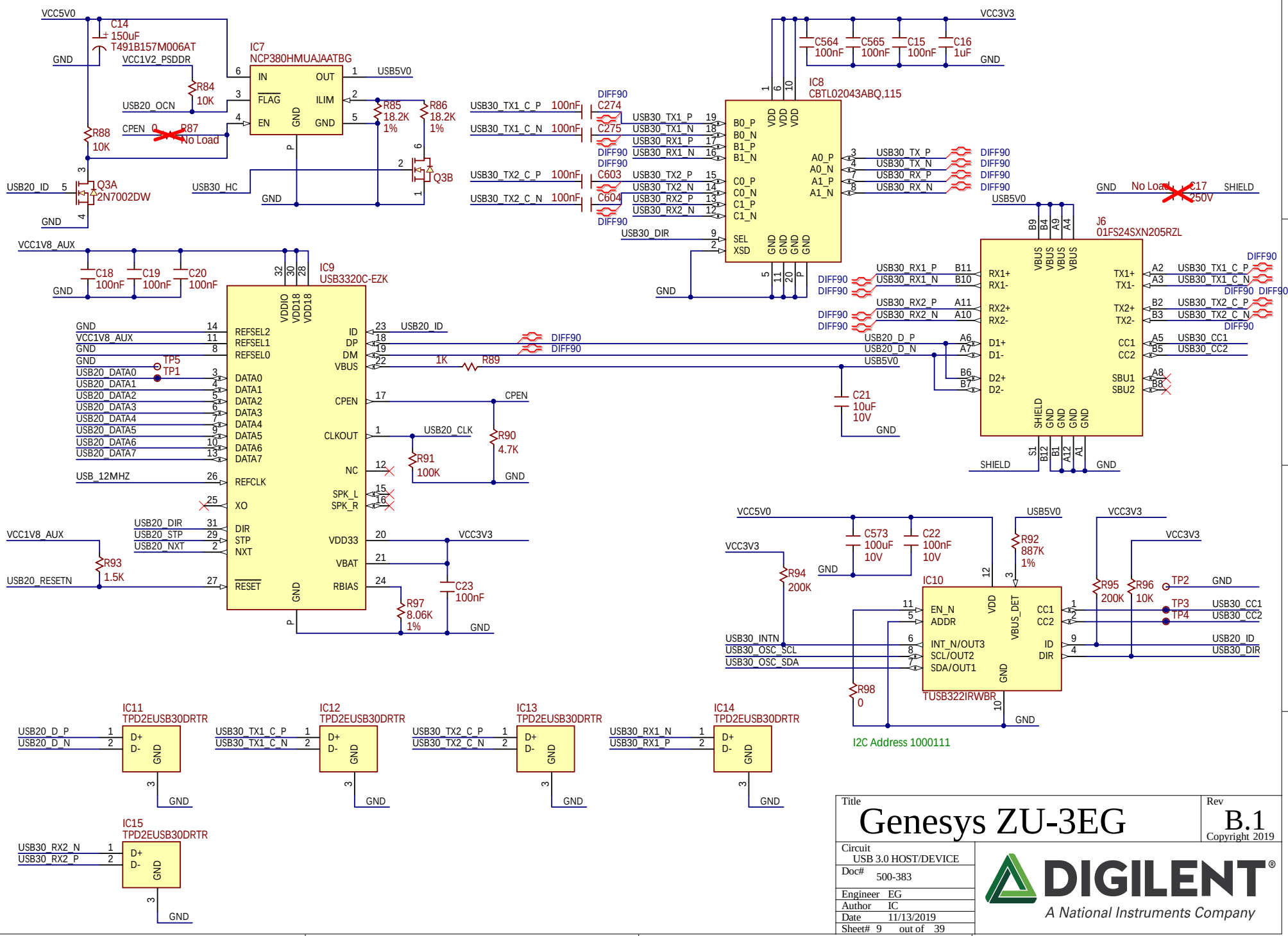
VCC5V0
C14
150uF
T491B157M006AT
GND
VCC1V2_PSDDR
R84
10K
USB20_OCN
CPEN
R87
No Load
R88
10K
USB20_ID
Q3A
2N7002DW
USB30_HC
IC7
NCP380HMUAJAATBG
IN
OUT
FLAG
ILIM
EN
GND
USB5V0
R85
18.2K
1%
R86
18.2K
1%
Q3B
VCC3V3
C564
100nF
C565
100nF
C15
100nF
C16
1uF
IC8
CBTL02043ABQ,115
USB30_TX1_C_P
USB30_TX1_C_N
USB30_TX2_C_P
USB30_TX2_C_N
100nF
DIFF90
C274
C275
C603
C604
USB30_TX1_P
USB30_TX1_N
USB30_RX1_P
USB30_RX1_N
USB30_TX2_P
USB30_TX2_N
USB30_RX2_P
USB30_RX2_N
USB30_DIR
B0_P
B0_N
B1_P
B1_N
C0_P
C0_N
C1_P
C1_N
SEL
XSD
A0_P
A0_N
A1_P
A1_N
USB30_TX_P
USB30_TX_N
USB30_RX_P
USB30_RX_N
GND
No Load
C17
250V
SHIELD
J6
01FS24SXN205RZL
VBUS
RX1+
RX1-
RX2+
RX2-
TX1+
TX1-
TX2+
TX2-
D1+
D1-
D2+
D2-
CC1
CC2
SBU1
SBU2
SHIELD
VCC1V8_AUX
C18
100nF
C19
100nF
C20
100nF
IC9
USB3320C-EZK
VDDIO
VDD18
VDD18
REFSEL2
REFSEL1
REFSEL0
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
REFCLK
XO
DIR
STP
NXT
RESET
ID
DP
DM
VBUS
CPEN
CLKOUT
NC
SPK_L
SPK_R
VDD33
VBAT
RBIAS
USB20_DATA0
USB20_DATA1
USB20_DATA2
USB20_DATA3
USB20_DATA4
USB20_DATA5
USB20_DATA6
USB20_DATA7
USB_12MHZ
USB20_DIR
USB20_STP
USB20_NXT
USB20_RESETN
USB20_CLK
TP5
TP1
1K
R89
C21
10uF
10V
R90
4.7K
R91
100K
R93
1.5K
R97
8.06K
1%
C23
100nF
USB20_D_P
USB20_D_N
VCC5V0
C573
100uF
10V
C22
100nF
10V
R92
887K
1%
R94
200K
IC10
TUSB322IRWBR
EN_N
ADDR
INT_N/OUT3
SCL/OUT2
SDA/OUT1
VDD
VBUS_DET
CC1
CC2
ID
DIR
R95
200K
R96
10K
TP2
TP3
TP4
R98
0
USB30_INTN
USB30_OSC_SCL
USB30_OSC_SDA
I2C Address 1000111
IC11
IC12
IC13
IC14
IC15
TPD2EUSB30DRTR
D+
D-
GND
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
USB 3.0 HOST/DEVICE
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
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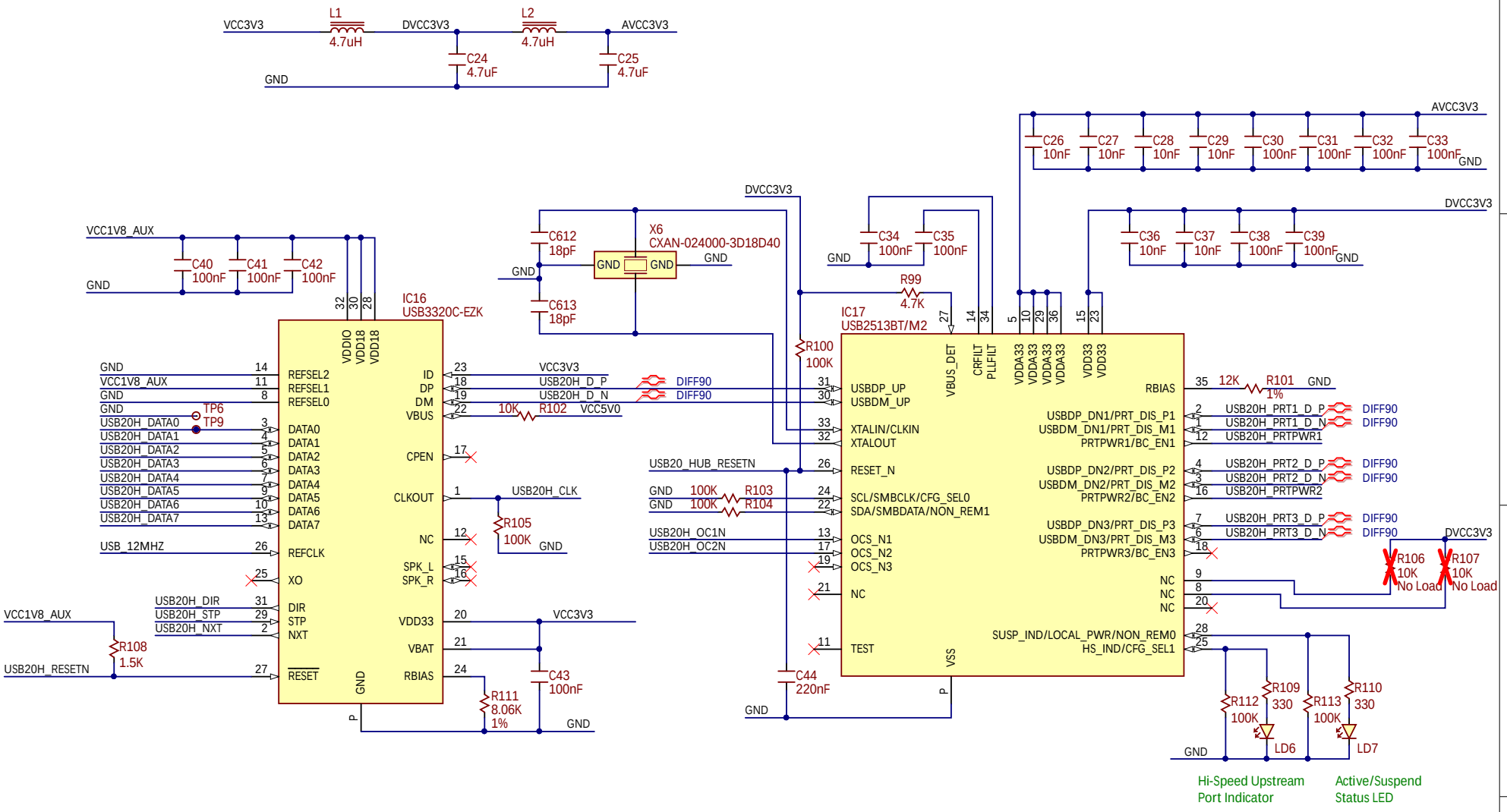

Title	Genesys ZU-3EG
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Circuit	USB 2.0 HOST PHY & HUB
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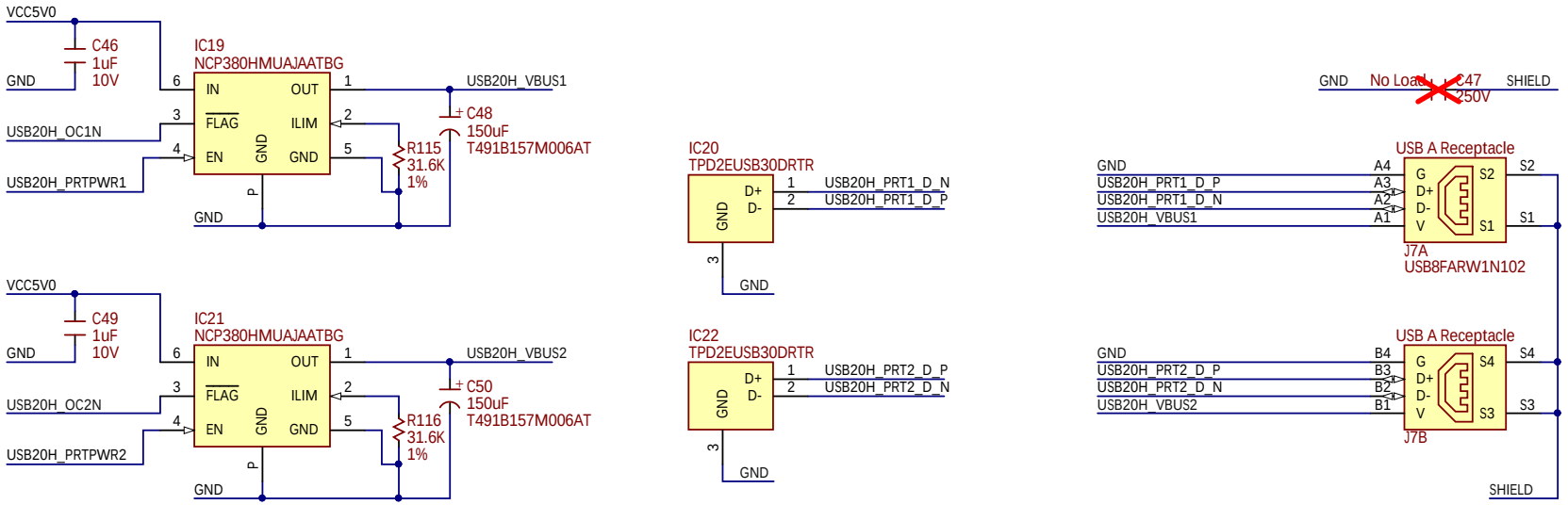

Title	Genesys ZU-3EG
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Circuit	USB 2.0 HUB CONN
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Doc#	500-383
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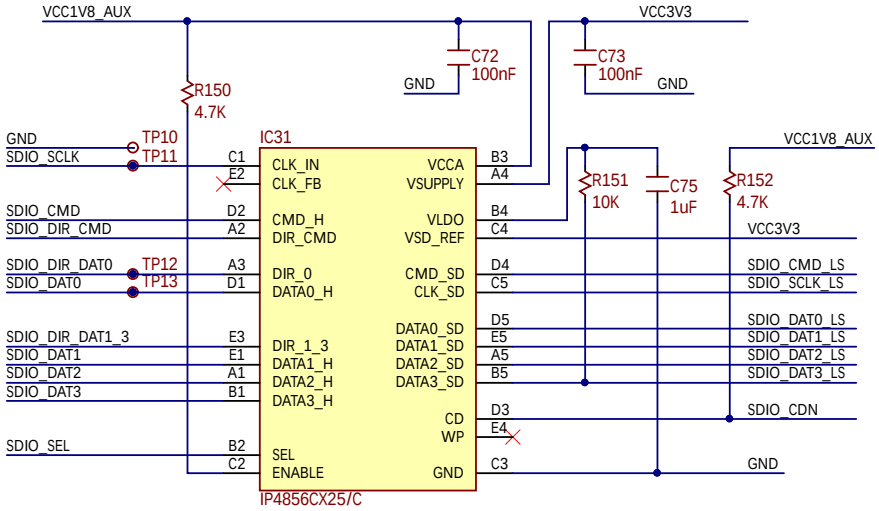

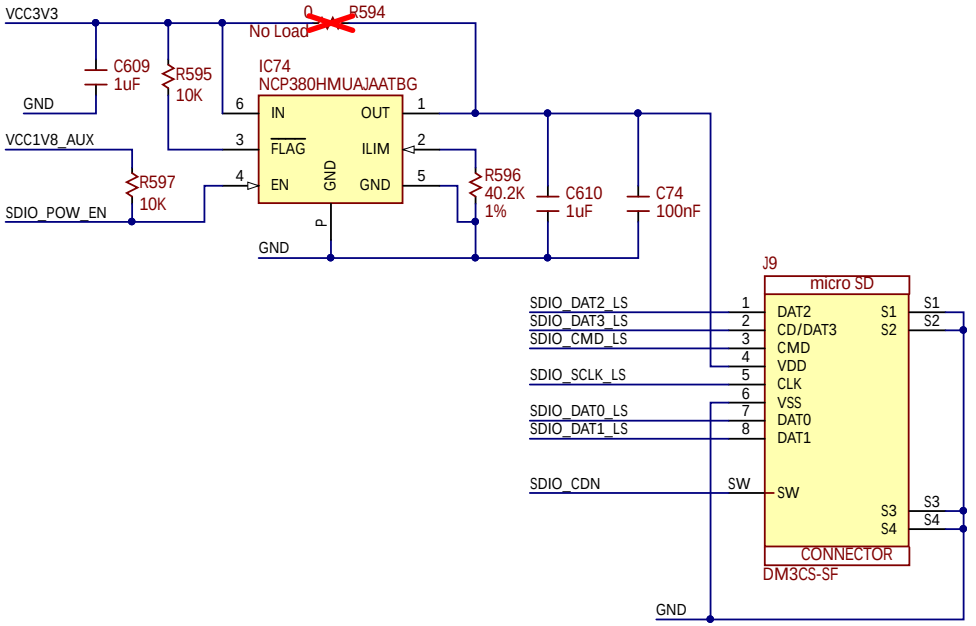

Title	Genesys ZU-3EG
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Circuit	SD CARD
Doc#	500-383
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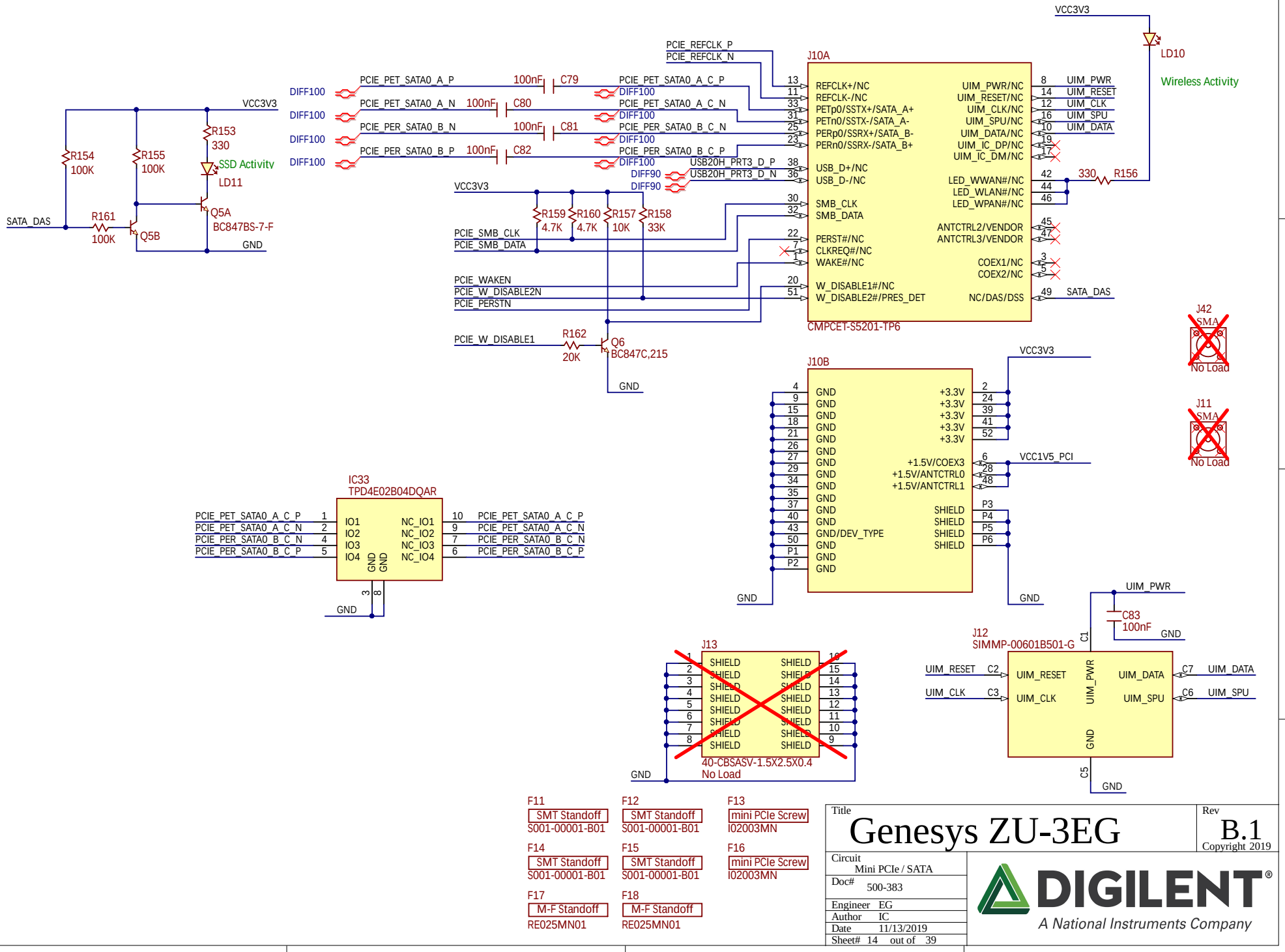
VCC3V3
R154 100K
R155 100K
R153 330
SSD Activity
LD11
Q5A BC847BS-7-F
Q5B
R161 100K
SATA_DAS
GND
PCIE_PET_SATA0_A_P
PCIE_PET_SATA0_A_N
PCIE_PER_SATA0_B_N
PCIE_PER_SATA0_B_P
DIFF100
100nF
C79
C80
C81
C82
PCIE_PET_SATA0_A_C_P
PCIE_PET_SATA0_A_C_N
PCIE_PER_SATA0_B_C_N
PCIE_PER_SATA0_B_C_P
PCIE_REFCLK_P
PCIE_REFCLK_N
J10A
REFCLK+/NC
REFCLK-/NC
PETp0/SSTX+/SATA_A+
PETn0/SSTX-/SATA_A-
PERp0/SSRX+/SATA_B-
PERn0/SSRX-/SATA_B+
USB_D+/NC
USB_D-/NC
SMB_CLK
SMB_DATA
PERST#/NC
CLKREQ#/NC
WAKE#/NC
W_DISABLE1#/NC
W_DISABLE2#/PRES_DET
UIM_PWR/NC
UIM_RESET/NC
UIM_CLK/NC
UIM_SPU/NC
UIM_DATA/NC
UIM_IC_DP/NC
UIM_IC_DM/NC
LED_WWAN#/NC
LED_WLAN#/NC
LED_WPAN#/NC
ANTCTRL2/VENDOR
ANTCTRL3/VENDOR
COEX1/NC
COEX2/NC
NC/DAS/DSS
CMPCET-S5201-TP6
USB20H_PRT3_D_P
USB20H_PRT3_D_N
DIFF90
R159 4.7K
R160 4.7K
R157 10K
R158 33K
PCIE_SMB_CLK
PCIE_SMB_DATA
PCIE_WAKEN
PCIE_W_DISABLE2N
PCIE_PERSTN
PCIE_W_DISABLE1
R162 20K
Q6 BC847C,215
LD10
Wireless Activity
R156 330
J42 SMA
No Load
J11 SMA
No Load
J10B
+3.3V
+1.5V/COEX3
+1.5V/ANTCTRL0
+1.5V/ANTCTRL1
SHIELD
GND/DEV_TYPE
VCC1V5_PCI
IC33 TPD4E02B04DQAR
IO1
IO2
IO3
IO4
NC_IO1
NC_IO2
NC_IO3
NC_IO4
J13
40-CBSASV-1.5X2.5X0.4
No Load
J12 SIMMP-00601B501-G
UIM_RESET
UIM_CLK
UIM_PWR
UIM_DATA
UIM_SPU
C83 100nF
C1
C2
C3
C5
C6
C7
F11 SMT Standoff S001-00001-B01
F12 SMT Standoff S001-00001-B01
F13 mini PCIe Screw I02003MN
F14 SMT Standoff S001-00001-B01
F15 SMT Standoff S001-00001-B01
F16 mini PCIe Screw I02003MN
F17 M-F Standoff RE025MN01
F18 M-F Standoff RE025MN01
Title
Genesys ZU-3EG
Rev
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Circuit
Mini PCIe / SATA
Doc#
500-383
Engineer EG
Author IC
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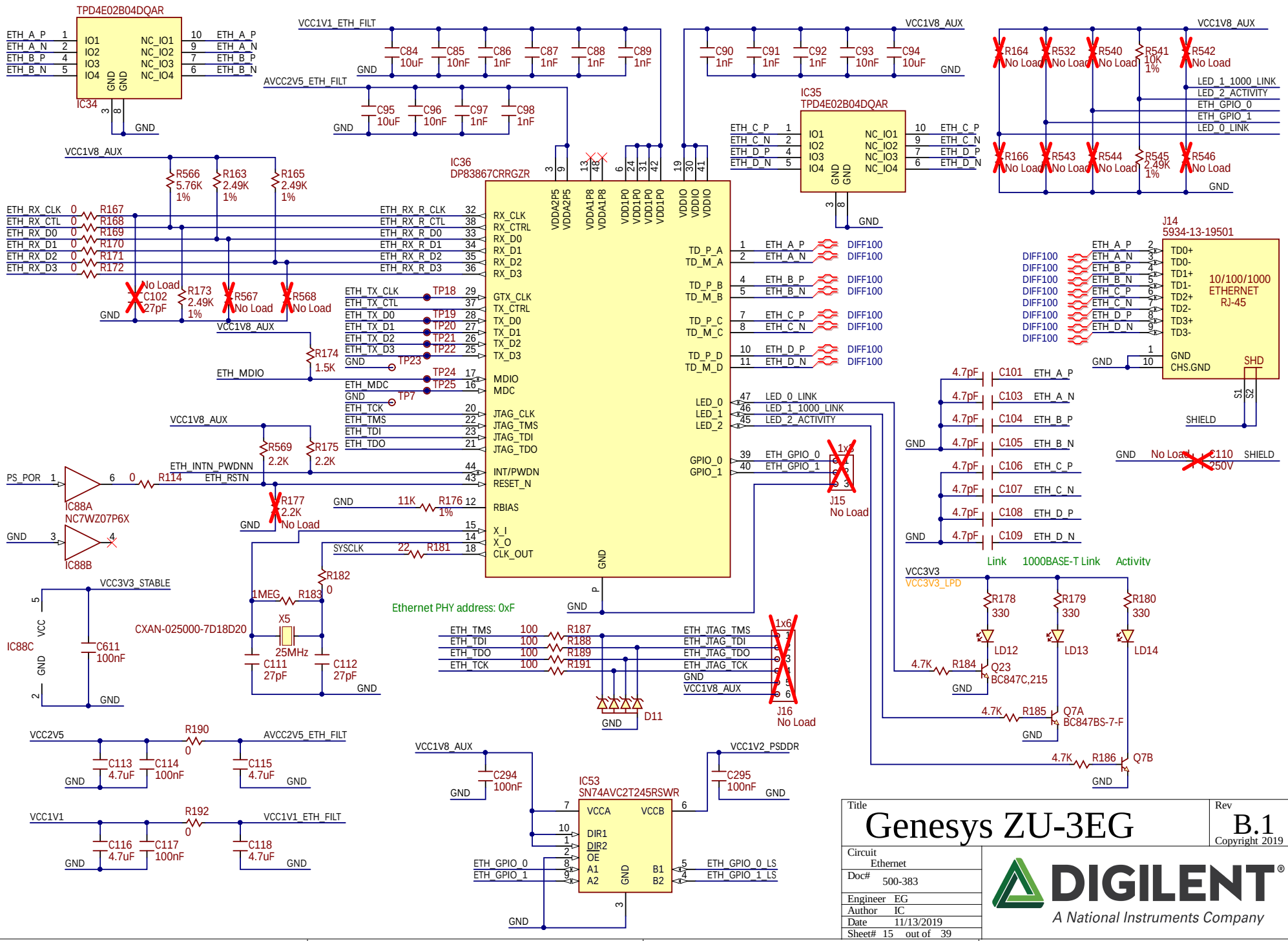
TPD4E02B04DQAR
IC34
IC35
IC36
DP83867CRRGZR
SN74AVC2T245RSWR
IC53
IC88A
NC7WZ07P6X
IC88B
IC88C
J14
5934-13-19501
10/100/1000
ETHERNET
RJ-45
J15
No Load
J16
No Load
D11
LD12
LD13
LD14
Q23
BC847C,215
Q7A
BC847BS-7-F
Q7B
CXAN-025000-7D18D20
25MHz
Ethernet PHY address: 0xF
Link
1000BASE-T Link
Activity
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
Ethernet
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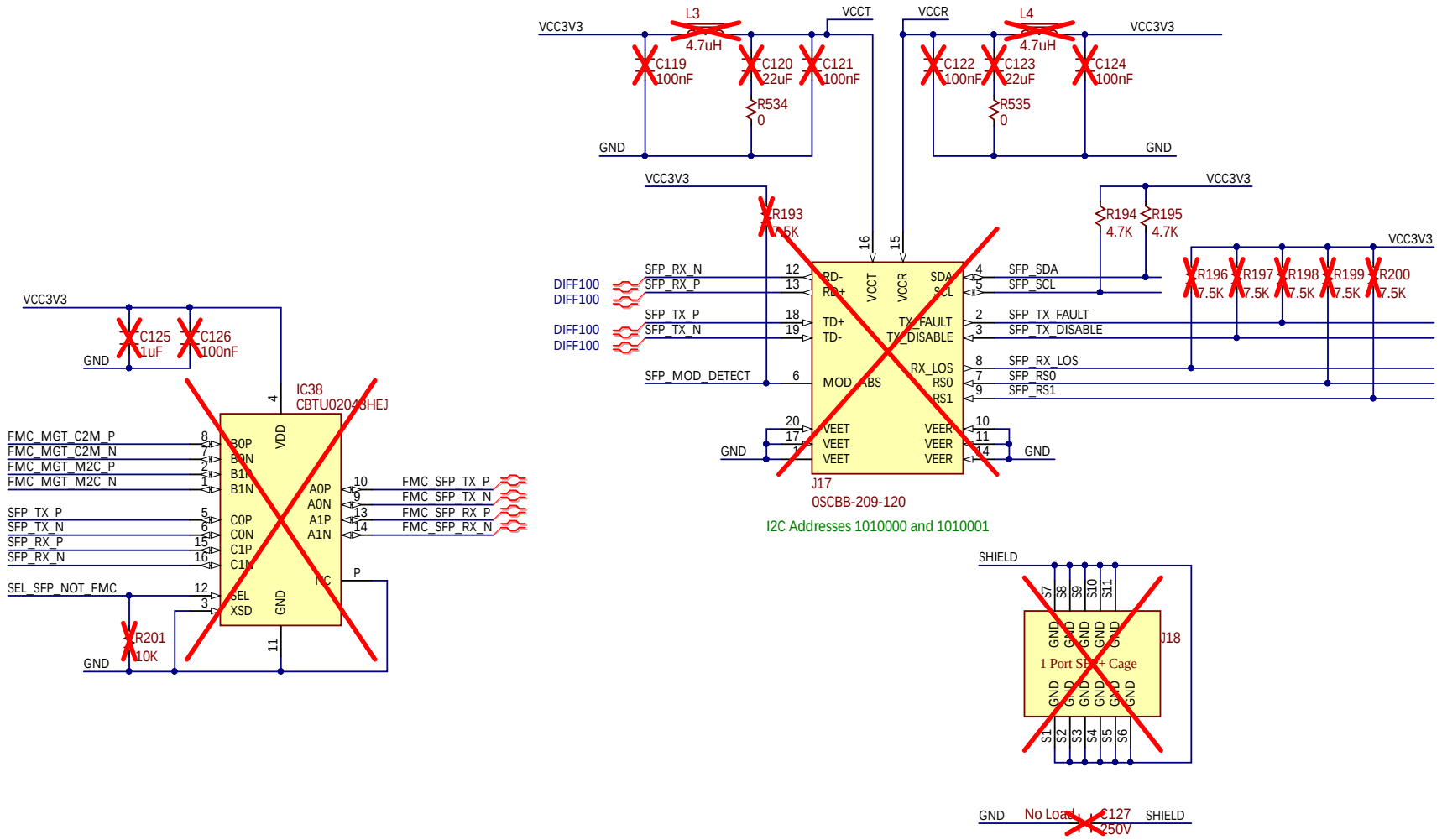

SFP+ cannot be used simultaneously with neither HDMI Source nor Sink due to the limited number of QPLL/CPLL primitives available in the GTH Quad.

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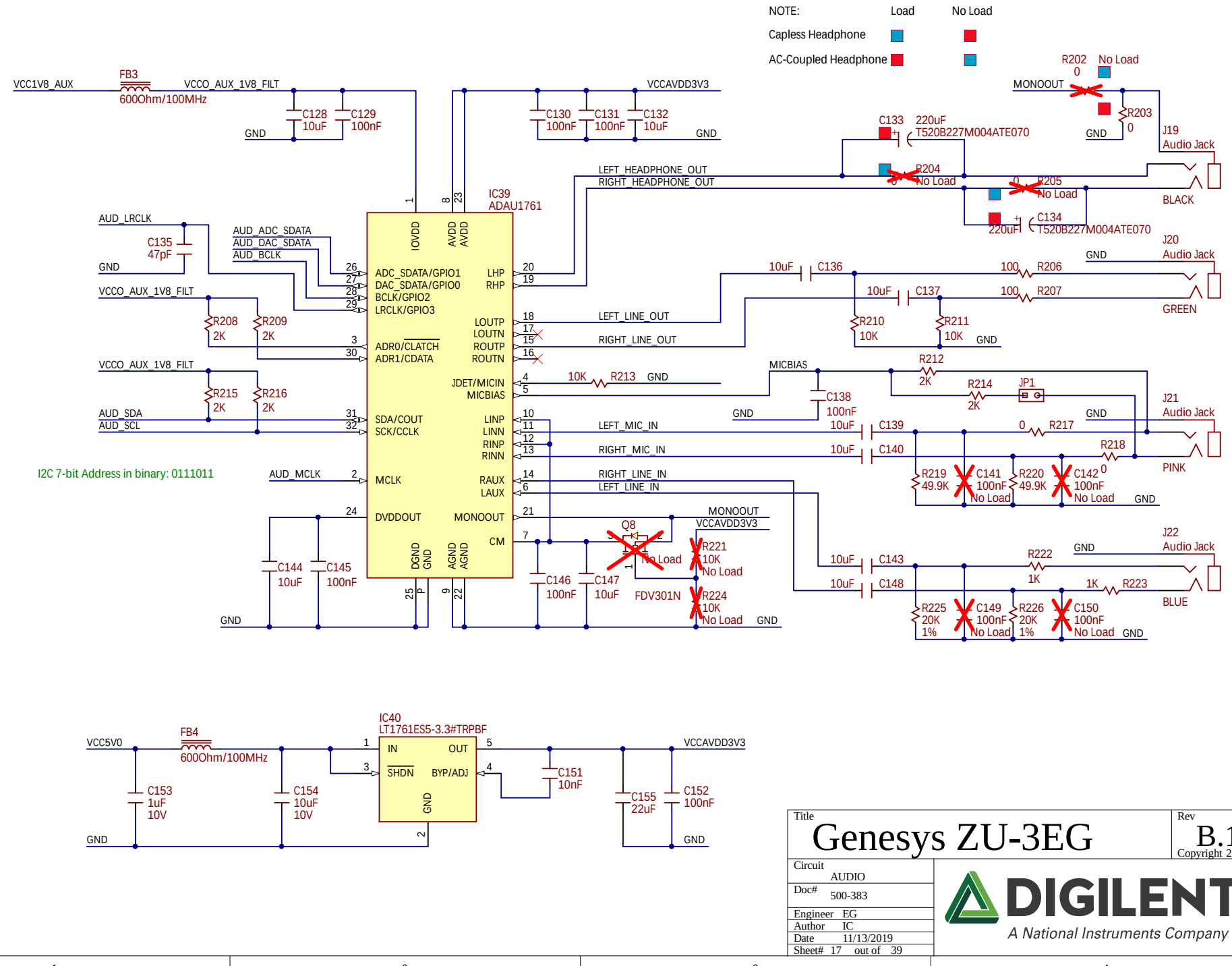

Title
Genesys ZU-3EG

Rev
B.1

Circuit	AUDIO
Doc#	500-383
Engineer	EG
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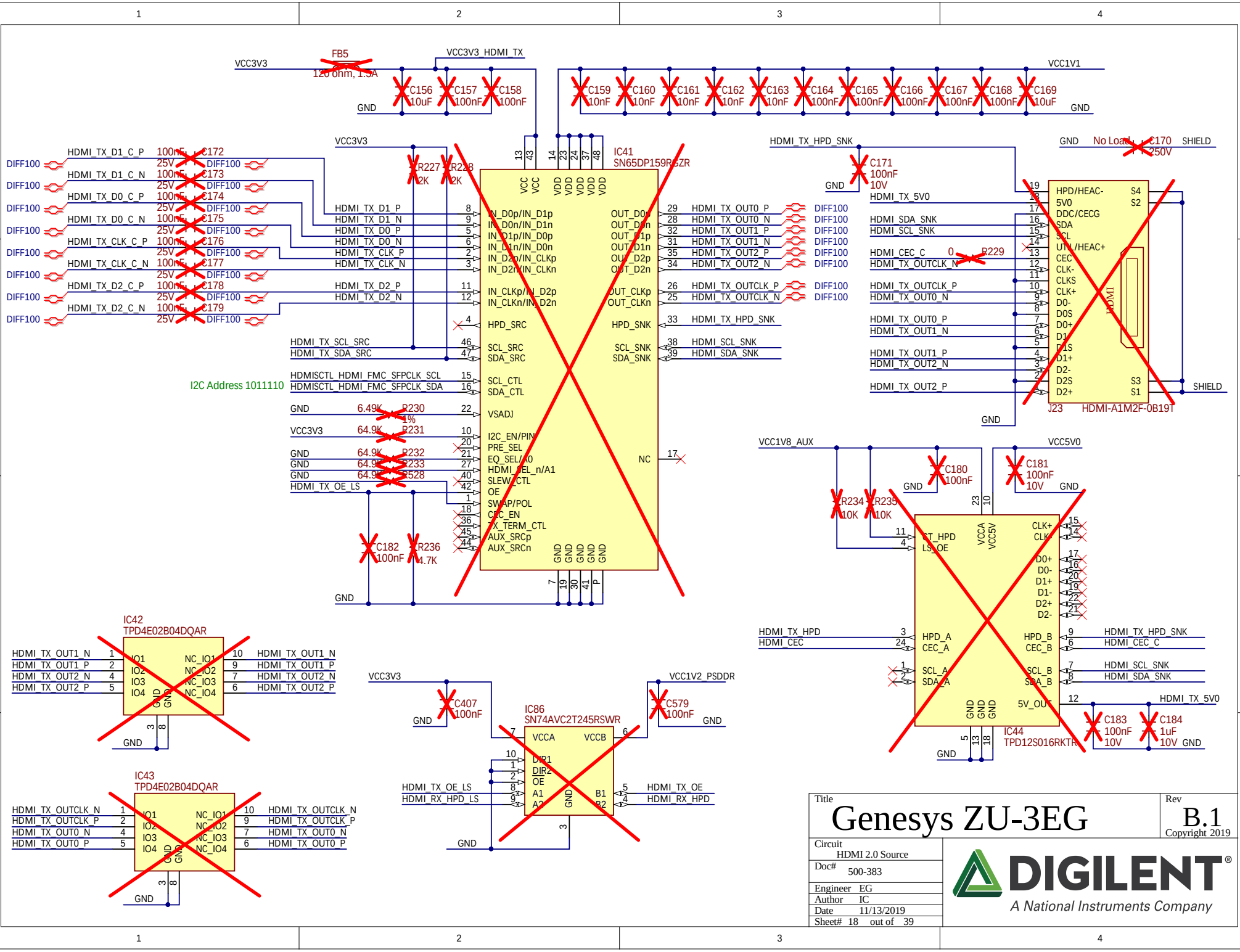
VCC3V3
FB5
120 ohm, 1.5A
VCC3V3_HDMI_TX
C156 10uF
C157 100nF
C158 100nF
GND
C159 10nF
C160 10nF
C161 10nF
C162 10nF
C163 10nF
C164 100nF
C165 100nF
C166 100nF
C167 100nF
C168 100nF
C169 10uF
VCC1V1
IC41
SN65DP159RGZR
HDMI_TX_D1_C_P
HDMI_TX_D1_C_N
HDMI_TX_D0_C_P
HDMI_TX_D0_C_N
HDMI_TX_CLK_C_P
HDMI_TX_CLK_C_N
HDMI_TX_D2_C_P
HDMI_TX_D2_C_N
DIFF100
100nF 25V
C172
C173
C174
C175
C176
C177
C178
C179
R227 2K
R228 2K
HDMI_TX_D1_P
HDMI_TX_D1_N
HDMI_TX_D0_P
HDMI_TX_D0_N
HDMI_TX_CLK_P
HDMI_TX_CLK_N
HDMI_TX_D2_P
HDMI_TX_D2_N
HDMI_TX_SCL_SRC
HDMI_TX_SDA_SRC
I2C Address 1011110
HDMISCTL_HDMI_FMC_SFPCLK_SCL
HDMISCTL_HDMI_FMC_SFPCLK_SDA
R230 6.49K 1%
R231 64.9K
R232 64.9K
R233 64.9K
R528 64.9K
HDMI_TX_OE_LS
C182 100nF
R236 4.7K
HDMI_TX_OUT0_P
HDMI_TX_OUT0_N
HDMI_TX_OUT1_P
HDMI_TX_OUT1_N
HDMI_TX_OUT2_P
HDMI_TX_OUT2_N
HDMI_TX_OUTCLK_P
HDMI_TX_OUTCLK_N
HDMI_TX_HPD_SNK
HDMI_SCL_SNK
HDMI_SDA_SNK
C171 100nF 10V
HDMI_TX_5V0
HDMI_CEC_C
R229 0
GND
No Load
C170 250V
SHIELD
J23
HDMI-A1M2F-0B19T
HDMI
IC42
TPD4E02B04DQAR
IC43
TPD4E02B04DQAR
VCC3V3
C407 100nF
IC86
SN74AVC2T245RSWR
VCC1V2_PSDDR
C579 100nF
HDMI_RX_HPD_LS
HDMI_TX_OE
HDMI_RX_HPD
VCC1V8_AUX
VCC5V0
C180 100nF
C181 100nF 10V
R234 10K
R235 10K
IC44
TPD12S016RKTR
HDMI_TX_HPD
HDMI_CEC
HDMI_CEC_C
HDMI_SCL_SNK
HDMI_SDA_SNK
C183 100nF 10V
C184 1uF 10V
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
HDMI 2.0 Source
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 18 out of 39
DIGILENT
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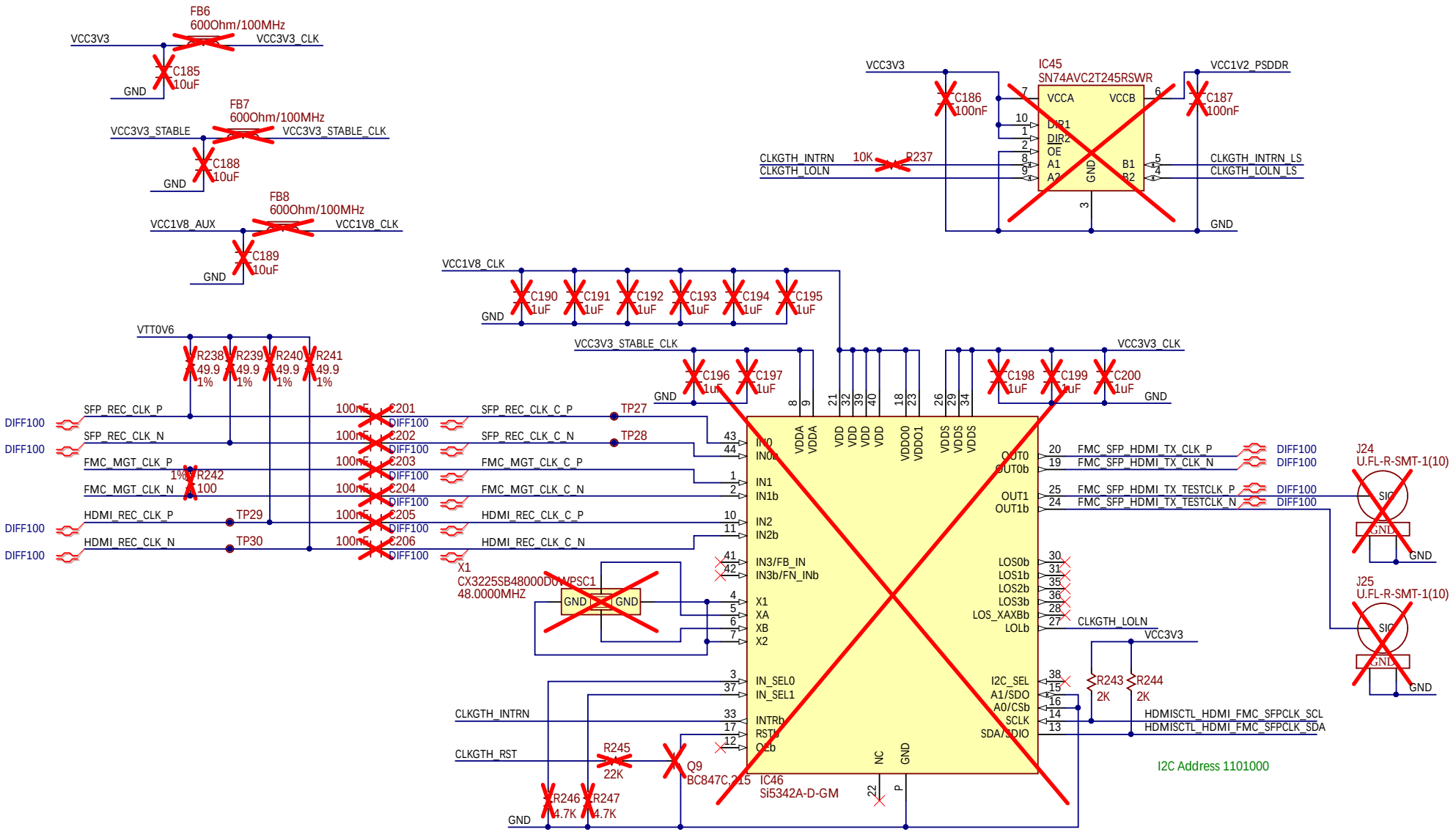

Upon board powerup, the first setting that must be done via I2C to the Si5342 is VDDIO level = 3.3V, by setting the IO_VDD_SEL bit to logic '1'.

Title	Genesys ZU-3EG
Rev	B.1
Copyright	2019
Circuit	FMC, SFP, HDMI Clock
Doc#	500-383
Engineer	EG
Author	IC
Date	11/13/2019
Sheet#	19 out of 39

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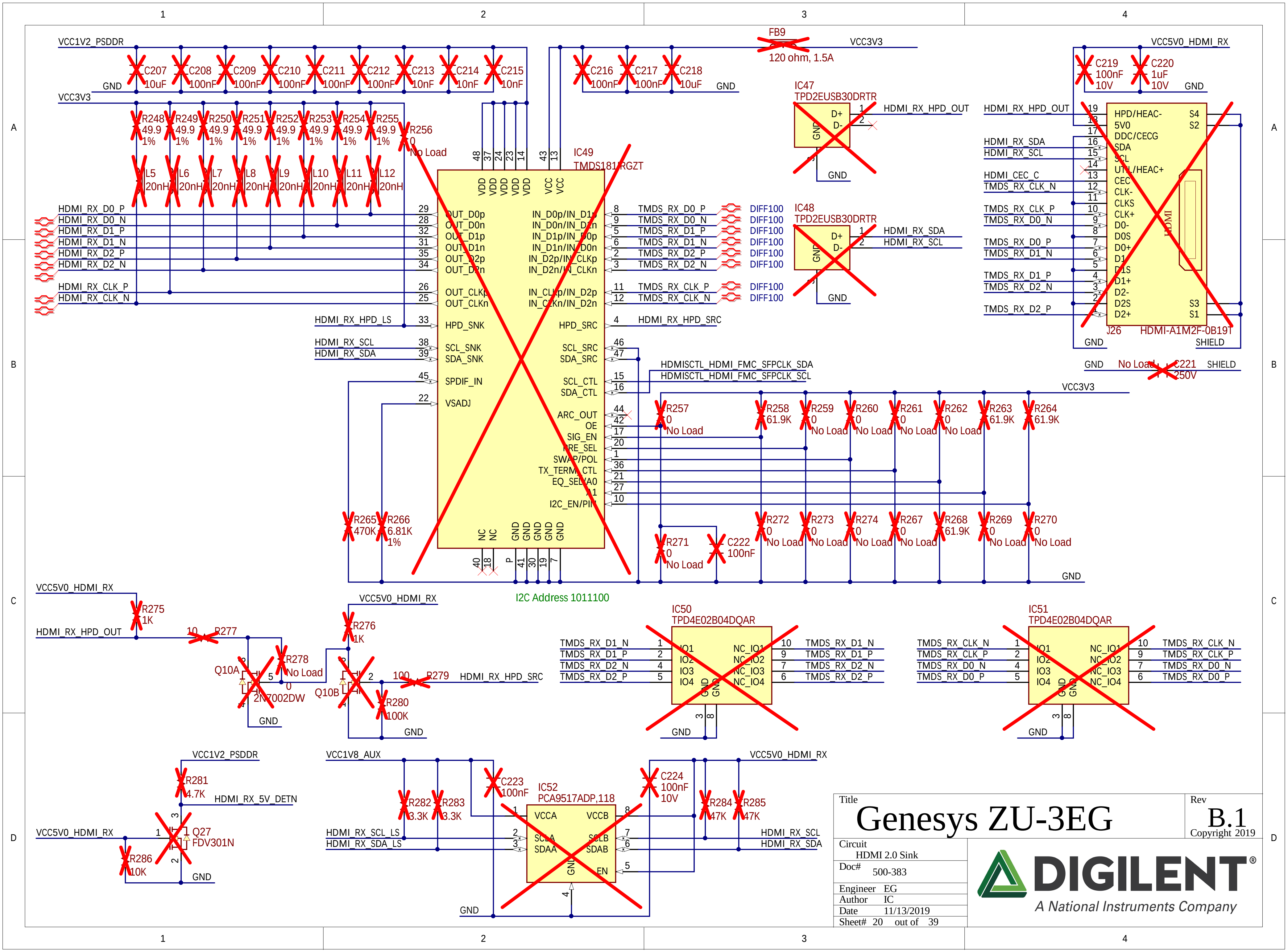
VCC1V2_PSDDR
VCC3V3
VCC5V0_HDMI_RX
FB9
120 ohm, 1.5A
C207 10uF
C208 100nF
C209 100nF
C210 100nF
C211 100nF
C212 100nF
C213 10nF
C214 10nF
C215 10nF
C216 100nF
C217 100nF
C218 10uF
C219 100nF 10V
C220 1uF 10V
GND
R248 49.9 1%
R249 49.9 1%
R250 49.9 1%
R251 49.9 1%
R252 49.9 1%
R253 49.9 1%
R254 49.9 1%
R255 49.9 1%
R256 0 No Load
L5 20nH
L6 20nH
L7 20nH
L8 20nH
L9 20nH
L10 20nH
L11 20nH
L12 20nH
HDMI_RX_D0_P
HDMI_RX_D0_N
HDMI_RX_D1_P
HDMI_RX_D1_N
HDMI_RX_D2_P
HDMI_RX_D2_N
HDMI_RX_CLK_P
HDMI_RX_CLK_N
HDMI_RX_HPD_LS
HDMI_RX_SCL
HDMI_RX_SDA
IC49
TMDS181IRGZT
VDD
VCC
OUT_D0p
OUT_D0n
OUT_D1p
OUT_D1n
OUT_D2p
OUT_D2n
OUT_CLKp
OUT_CLKn
HPD_SNK
SCL_SNK
SDA_SNK
SPDIF_IN
VSADJ
IN_D0p/IN_D1n
IN_D0n/IN_D2n
IN_D1p/IN_D0p
IN_D1n/IN_D0n
IN_D2p/IN_CLKp
IN_D2n/IN_CLKn
IN_CLKp/IN_D2p
IN_CLKn/IN_D2n
HPD_SRC
SCL_SRC
SDA_SRC
SCL_CTL
SDA_CTL
ARC_OUT
OE
SIG_EN
PRE_SEL
SWAP/POL
TX_TERM_CTL
EQ_SEL/A0
A1
I2C_EN/PIN
NC
GND
TMDS_RX_D0_P
TMDS_RX_D0_N
TMDS_RX_D1_P
TMDS_RX_D1_N
TMDS_RX_D2_P
TMDS_RX_D2_N
TMDS_RX_CLK_P
TMDS_RX_CLK_N
DIFF100
HDMI_RX_HPD_SRC
HDMISCTL_HDMI_FMC_SFPCLK_SDA
HDMISCTL_HDMI_FMC_SFPCLK_SCL
IC47
TPD2EUSB30DRTR
IC48
TPD2EUSB30DRTR
D+
D-
HDMI_RX_HPD_OUT
HDMI_RX_CEC_C
J26
HDMI-A1M2F-0B19T
HPD/HEAC-
5V0
DDC/CECG
SDA
SCL
UTIL/HEAC+
CEC
CLK-
CLKS
CLK+
D0-
D0S
D0+
D1-
D1S
D1+
D2-
D2S
D2+
S1
S2
S3
S4
SHIELD
HDMI
C221 No Load 250V
R257 0 No Load
R258 61.9K
R259 0 No Load
R260 0 No Load
R261 0 No Load
R262 0 No Load
R263 61.9K
R264 61.9K
R265 470K
R266 6.81K 1%
R271 0 No Load
C222 100nF
R272 0 No Load
R273 0 No Load
R274 0 No Load
R267 0 No Load
R268 61.9K
R269 0 No Load
R270 0 No Load
I2C Address 1011100
R275 1K
R277 10
R278 0 No Load
Q10A
2N7002DW
R276 1K
Q10B
R279 100
R280 100K
IC50
TPD4E02B04DQAR
IC51
TPD4E02B04DQAR
IO1
IO2
IO3
IO4
NC_IO1
NC_IO2
NC_IO3
NC_IO4
VCC1V8_AUX
R281 4.7K
HDMI_RX_5V_DETN
Q27
FDV301N
R286 10K
R282 3.3K
R283 3.3K
C223 100nF
IC52
PCA9517ADP,118
VCCA
VCCB
SCLA
SDAA
SCLB
SDAB
EN
C224 100nF 10V
R284 47K
R285 47K
HDMI_RX_SCL_LS
HDMI_RX_SDA_LS

Title: Genesys ZU-3EG

Rev: B.1

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Circuit: HDMI 2.0 Sink

Doc#: 500-383

Engineer: EG

Author: IC

Date: 11/13/2019

Sheet# 20 out of 39

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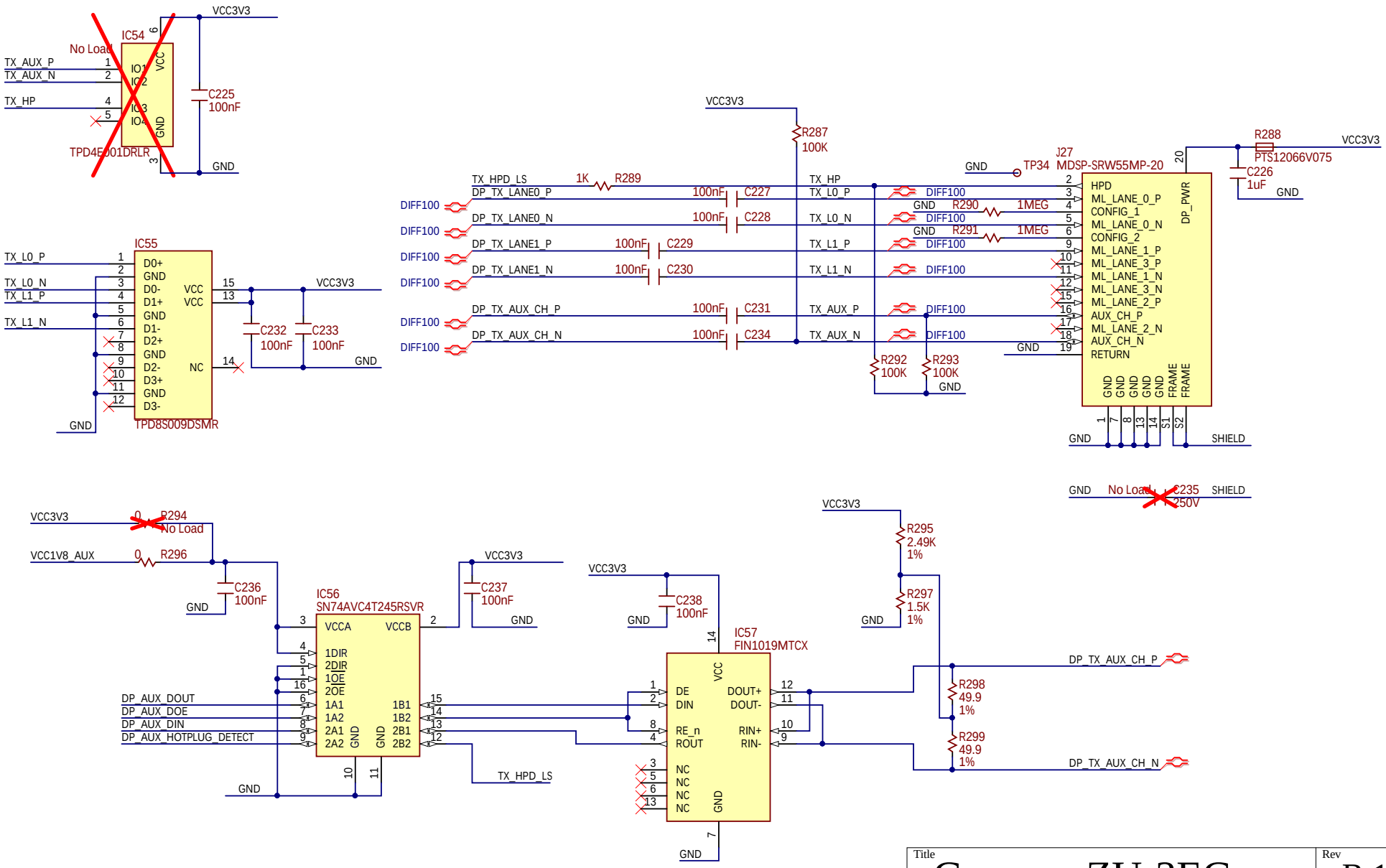

Title	Genesys ZU-3EG
Rev	B.1
Copyright	2019
Circuit	DisplayPort Source
Doc#	500-383
Engineer	EG
Author	IC
Date	11/13/2019
Sheet#	21 out of 39

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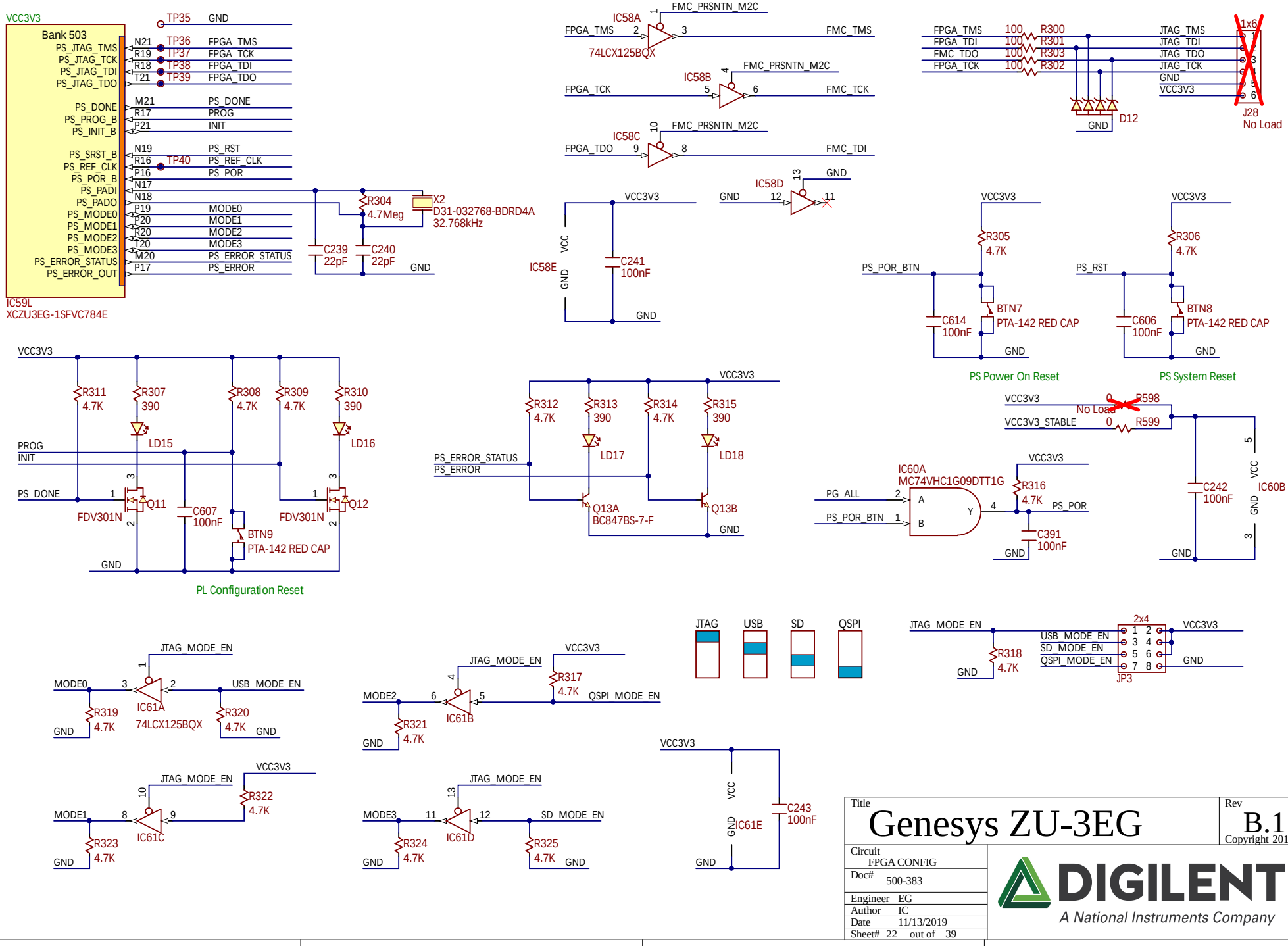
VCC3V3
Bank 503
PS_JTAG_TMS
PS_JTAG_TCK
PS_JTAG_TDI
PS_JTAG_TDO
PS_DONE
PS_PROG_B
PS_INIT_B
PS_SRST_B
PS_REF_CLK
PS_POR_B
PS_PADI
PS_PADO
PS_MODE0
PS_MODE1
PS_MODE2
PS_MODE3
PS_ERROR_STATUS
PS_ERROR_OUT
IC59L
XCZU3EG-1SFVC784E
TP35 GND
TP36 FPGA_TMS
TP37 FPGA_TCK
TP38 FPGA_TDI
TP39 FPGA_TDO
PS_DONE
PROG
INIT
PS_RST
TP40 PS_REF_CLK
PS_POR
MODE0
MODE1
MODE2
MODE3
PS_ERROR_STATUS
PS_ERROR
R304 4.7Meg
X2
D31-032768-BDRD4A
32.768kHz
C239 22pF
C240 22pF
GND
IC58A
74LCX125BQX
FMC_PRSNTN_M2C
FPGA_TMS
FMC_TMS
IC58B
FPGA_TCK
FMC_TCK
IC58C
FPGA_TDO
FMC_TDI
IC58D
IC58E
C241 100nF
FPGA_TMS 100 R300
FPGA_TDI 100 R301
FMC_TDO 100 R303
FPGA_TCK 100 R302
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TCK
D12
1x6
J28
No Load
R305 4.7K
R306 4.7K
PS_POR_BTN
PS_RST
BTN7
PTA-142 RED CAP
BTN8
C614 100nF
C606 100nF
PS Power On Reset
PS System Reset
R311 4.7K
R307 390
R308 4.7K
R309 4.7K
R310 390
LD15
LD16
PROG
INIT
PS_DONE
Q11
Q12
FDV301N
C607 100nF
BTN9
PTA-142 RED CAP
PL Configuration Reset
R312 4.7K
R313 390
R314 4.7K
R315 390
LD17
LD18
PS_ERROR_STATUS
PS_ERROR
Q13A
BC847BS-7-F
Q13B
R598 No Load
R599 0
VCC3V3_STABLE
IC60A
MC74VHC1G09DTT1G
PG_ALL
PS_POR_BTN
R316 4.7K
PS_POR
C391 100nF
C242 100nF
IC60B
JTAG
USB
SD
QSPI
JTAG_MODE_EN
R318 4.7K
2x4
USB_MODE_EN
SD_MODE_EN
QSPI_MODE_EN
JP3
MODE0
IC61A
74LCX125BQX
R319 4.7K
R320 4.7K
MODE2
IC61B
R321 4.7K
R317 4.7K
MODE1
IC61C
R323 4.7K
R322 4.7K
MODE3
IC61D
R324 4.7K
R325 4.7K
IC61E
C243 100nF
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
FPGA CONFIG
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 22 out of 39
DIGILENT
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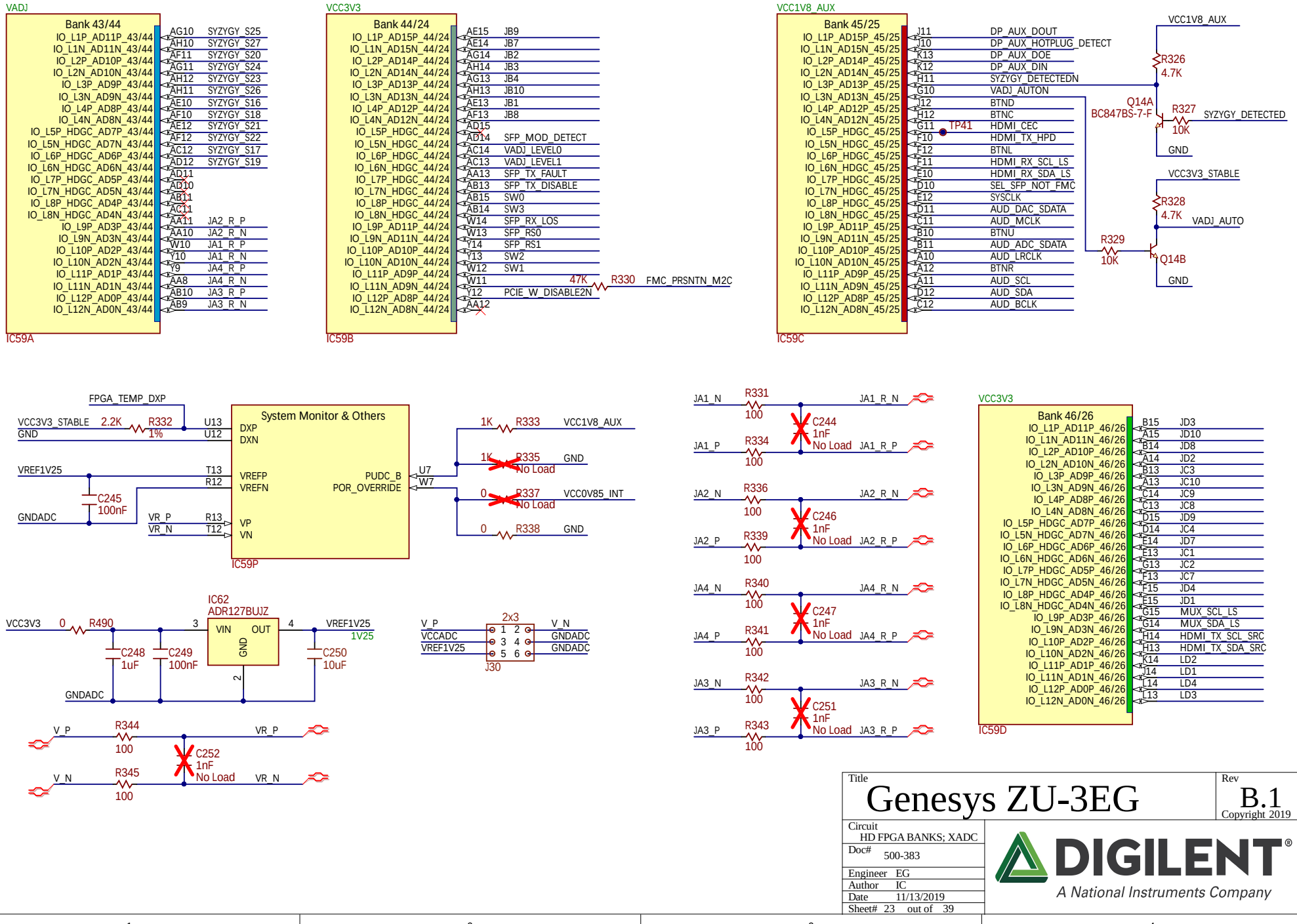
VADJ
Bank 43/44
IO_L1P_AD11P_43/44
IO_L1N_AD11N_43/44
IO_L2P_AD10P_43/44
IO_L2N_AD10N_43/44
IO_L3P_AD9P_43/44
IO_L3N_AD9N_43/44
IO_L4P_AD8P_43/44
IO_L4N_AD8N_43/44
IO_L5P_HDGC_AD7P_43/44
IO_L5N_HDGC_AD7N_43/44
IO_L6P_HDGC_AD6P_43/44
IO_L6N_HDGC_AD6N_43/44
IO_L7P_HDGC_AD5P_43/44
IO_L7N_HDGC_AD5N_43/44
IO_L8P_HDGC_AD4P_43/44
IO_L8N_HDGC_AD4N_43/44
IO_L9P_AD3P_43/44
IO_L9N_AD3N_43/44
IO_L10P_AD2P_43/44
IO_L10N_AD2N_43/44
IO_L11P_AD1P_43/44
IO_L11N_AD1N_43/44
IO_L12P_AD0P_43/44
IO_L12N_AD0N_43/44
AG10 SYZYGY_S25
AH10 SYZYGY_S27
AF11 SYZYGY_S20
AG11 SYZYGY_S24
AH12 SYZYGY_S23
AH11 SYZYGY_S26
AE10 SYZYGY_S16
AF10 SYZYGY_S18
AE12 SYZYGY_S21
AF12 SYZYGY_S22
AC12 SYZYGY_S17
AD12 SYZYGY_S19
AD11
AD10
AB11
AC11
AA11 JA2_R_P
AA10 JA2_R_N
W10 JA1_R_P
Y10 JA1_R_N
Y9 JA4_R_P
AA8 JA4_R_N
AB10 JA3_R_P
AB9 JA3_R_N
IC59A
VCC3V3
Bank 44/24
IO_L1P_AD15P_44/24
IO_L1N_AD15N_44/24
IO_L2P_AD14P_44/24
IO_L2N_AD14N_44/24
IO_L3P_AD13P_44/24
IO_L3N_AD13N_44/24
IO_L4P_AD12P_44/24
IO_L4N_AD12N_44/24
IO_L5P_HDGC_44/24
IO_L5N_HDGC_44/24
IO_L6P_HDGC_44/24
IO_L6N_HDGC_44/24
IO_L7P_HDGC_44/24
IO_L7N_HDGC_44/24
IO_L8P_HDGC_44/24
IO_L8N_HDGC_44/24
IO_L9P_AD11P_44/24
IO_L9N_AD11N_44/24
IO_L10P_AD10P_44/24
IO_L10N_AD10N_44/24
IO_L11P_AD9P_44/24
IO_L11N_AD9N_44/24
IO_L12P_AD8P_44/24
IO_L12N_AD8N_44/24
AE15 JB9
AE14 JB7
AG14 JB2
AH14 JB3
AG13 JB4
AH13 JB10
AE13 JB1
AF13 JB8
AD15
AD14 SFP_MOD_DETECT
AC14 VADJ_LEVEL0
AC13 VADJ_LEVEL1
AA13 SFP_TX_FAULT
AB13 SFP_TX_DISABLE
AB15 SW0
AB14 SW3
W14 SFP_RX_LOS
W13 SFP_RS0
Y14 SFP_RS1
Y13 SW2
W12 SW1
W11
Y12 PCIE_W_DISABLE2N
AA12
47K R330 FMC_PRSNTN_M2C
IC59B
VCC1V8_AUX
Bank 45/25
IO_L1P_AD15P_45/25
IO_L1N_AD15N_45/25
IO_L2P_AD14P_45/25
IO_L2N_AD14N_45/25
IO_L3P_AD13P_45/25
IO_L3N_AD13N_45/25
IO_L4P_AD12P_45/25
IO_L4N_AD12N_45/25
IO_L5P_HDGC_45/25
IO_L5N_HDGC_45/25
IO_L6P_HDGC_45/25
IO_L6N_HDGC_45/25
IO_L7P_HDGC_45/25
IO_L7N_HDGC_45/25
IO_L8P_HDGC_45/25
IO_L8N_HDGC_45/25
IO_L9P_AD11P_45/25
IO_L9N_AD11N_45/25
IO_L10P_AD10P_45/25
IO_L10N_AD10N_45/25
IO_L11P_AD9P_45/25
IO_L11N_AD9N_45/25
IO_L12P_AD8P_45/25
IO_L12N_AD8N_45/25
J11 DP_AUX_DOUT
J10 DP_AUX_HOTPLUG_DETECT
K13 DP_AUX_DOE
K12 DP_AUX_DIN
H11 SYZYGY_DETECTEDN
G10 VADJ_AUTON
J12 BTND
H12 BTNC
G11 HDMI_CEC
F10 HDMI_TX_HPD
F12 BTNL
F11 HDMI_RX_SCL_LS
E10 HDMI_RX_SDA_LS
D10 SEL_SFP_NOT_FMC
E12 SYSCLK
D11 AUD_DAC_SDATA
C11 AUD_MCLK
B10 BTNU
B11 AUD_ADC_SDATA
A10 AUD_LRCLK
A12 BTNR
A11 AUD_SCL
D12 AUD_SDA
C12 AUD_BCLK
TP41
IC59C
VCC1V8_AUX
R326
4.7K
Q14A
BC847BS-7-F
R327
10K
SYZYGY_DETECTED
GND
VCC3V3_STABLE
R328
4.7K
VADJ_AUTO
R329
10K
Q14B
GND
FPGA_TEMP_DXP
System Monitor & Others
VCC3V3_STABLE
2.2K
R332
1%
U13
U12
GND
DXP
DXN
VREF1V25
T13
R12
VREFP
VREFN
C245
100nF
GNDADC
VR_P
VR_N
R13
T12
VP
VN
PUDC_B
POR_OVERRIDE
U7
W7
IC59P
1K R333 VCC1V8_AUX
1K R335 GND
No Load
0 R337 VCC0V85_INT
No Load
0 R338 GND
JA1_N
JA1_P
JA2_N
JA2_P
JA4_N
JA4_P
JA3_N
JA3_P
R331
R334
R336
R339
R340
R341
R342
R343
100
C244
C246
C247
C251
1nF
No Load
JA1_R_N
JA1_R_P
JA2_R_N
JA2_R_P
JA4_R_N
JA4_R_P
JA3_R_N
JA3_R_P
VCC3V3
Bank 46/26
IO_L1P_AD11P_46/26
IO_L1N_AD11N_46/26
IO_L2P_AD10P_46/26
IO_L2N_AD10N_46/26
IO_L3P_AD9P_46/26
IO_L3N_AD9N_46/26
IO_L4P_AD8P_46/26
IO_L4N_AD8N_46/26
IO_L5P_HDGC_AD7P_46/26
IO_L5N_HDGC_AD7N_46/26
IO_L6P_HDGC_AD6P_46/26
IO_L6N_HDGC_AD6N_46/26
IO_L7P_HDGC_AD5P_46/26
IO_L7N_HDGC_AD5N_46/26
IO_L8P_HDGC_AD4P_46/26
IO_L8N_HDGC_AD4N_46/26
IO_L9P_AD3P_46/26
IO_L9N_AD3N_46/26
IO_L10P_AD2P_46/26
IO_L10N_AD2N_46/26
IO_L11P_AD1P_46/26
IO_L11N_AD1N_46/26
IO_L12P_AD0P_46/26
IO_L12N_AD0N_46/26
B15 JD3
A15 JD10
B14 JD8
A14 JD2
B13 JC3
A13 JC10
C14 JC9
C13 JC8
D15 JD9
D14 JC4
E14 JD7
E13 JC1
G13 JC2
F13 JC7
F15 JD4
E15 JD1
G15 MUX_SCL_LS
G14 MUX_SDA_LS
H14 HDMI_TX_SCL_SRC
H13 HDMI_TX_SDA_SRC
K14 LD2
J14 LD1
L14 LD4
L13 LD3
IC59D
IC62
ADR127BUJZ
VCC3V3
0 R490
VIN
OUT
GND
VREF1V25
1V25
C248
1uF
C249
100nF
C250
10uF
GNDADC
V_P
V_N
2x3
VCCADC
VREF1V25
GNDADC
GNDADC
J30
R344
R345
100
C252
1nF
No Load
VR_P
VR_N
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
HD FPGA BANKS; XADC
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 23 out of 39
DIGILENT
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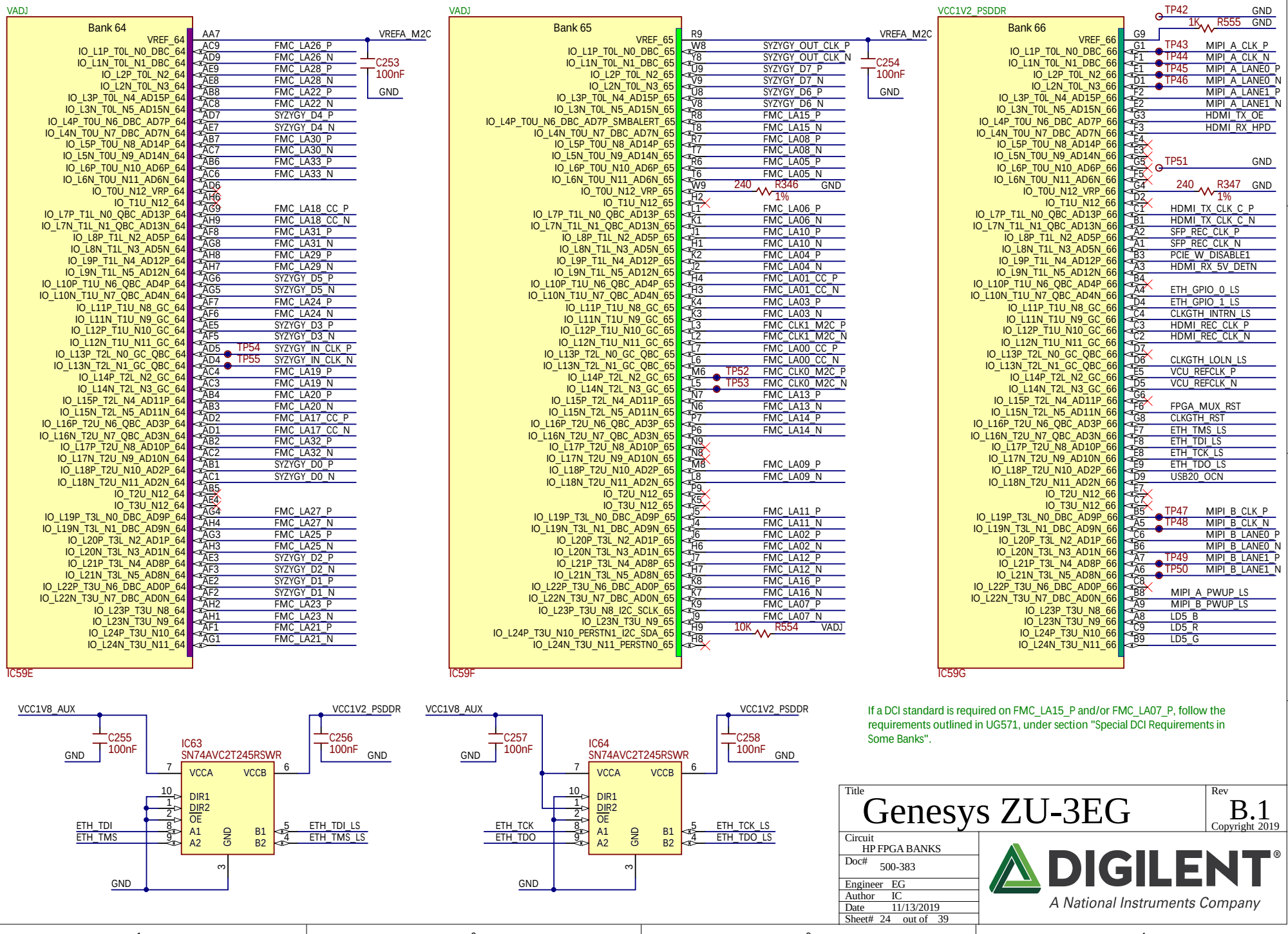
VADJ
Bank 64
IC59E
VADJ
Bank 65
IC59F
VCC1V2_PSDDR
Bank 66
IC59G
VCC1V8_AUX
VCC1V2_PSDDR
IC63
SN74AVC2T245RSWR
IC64
SN74AVC2T245RSWR
If a DCI standard is required on FMC_LA15_P and/or FMC_LA07_P, follow the requirements outlined in UG571, under section "Special DCI Requirements in Some Banks".
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
HP FPGA BANKS
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 24 out of 39
DIGILENT
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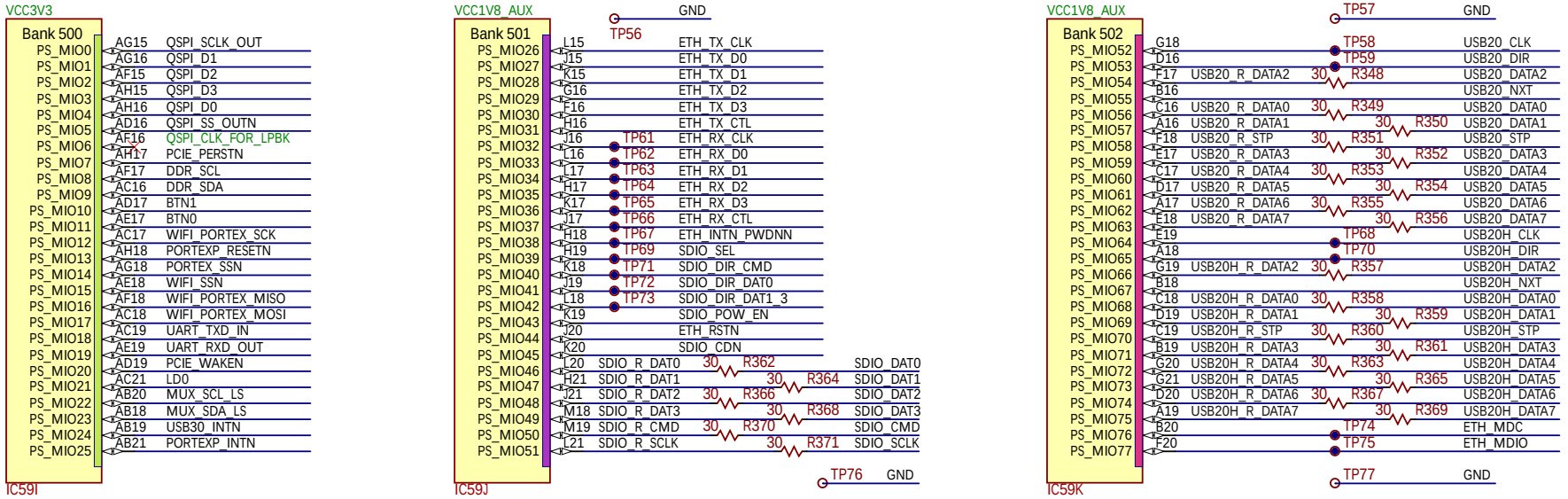

Title: Genesys ZU-3EG

Rev: B.1

Circuit: MIO BANKS; SPI FLASH

Doc# 500-383

Engineer EG

Author IC

Date 11/13/2019

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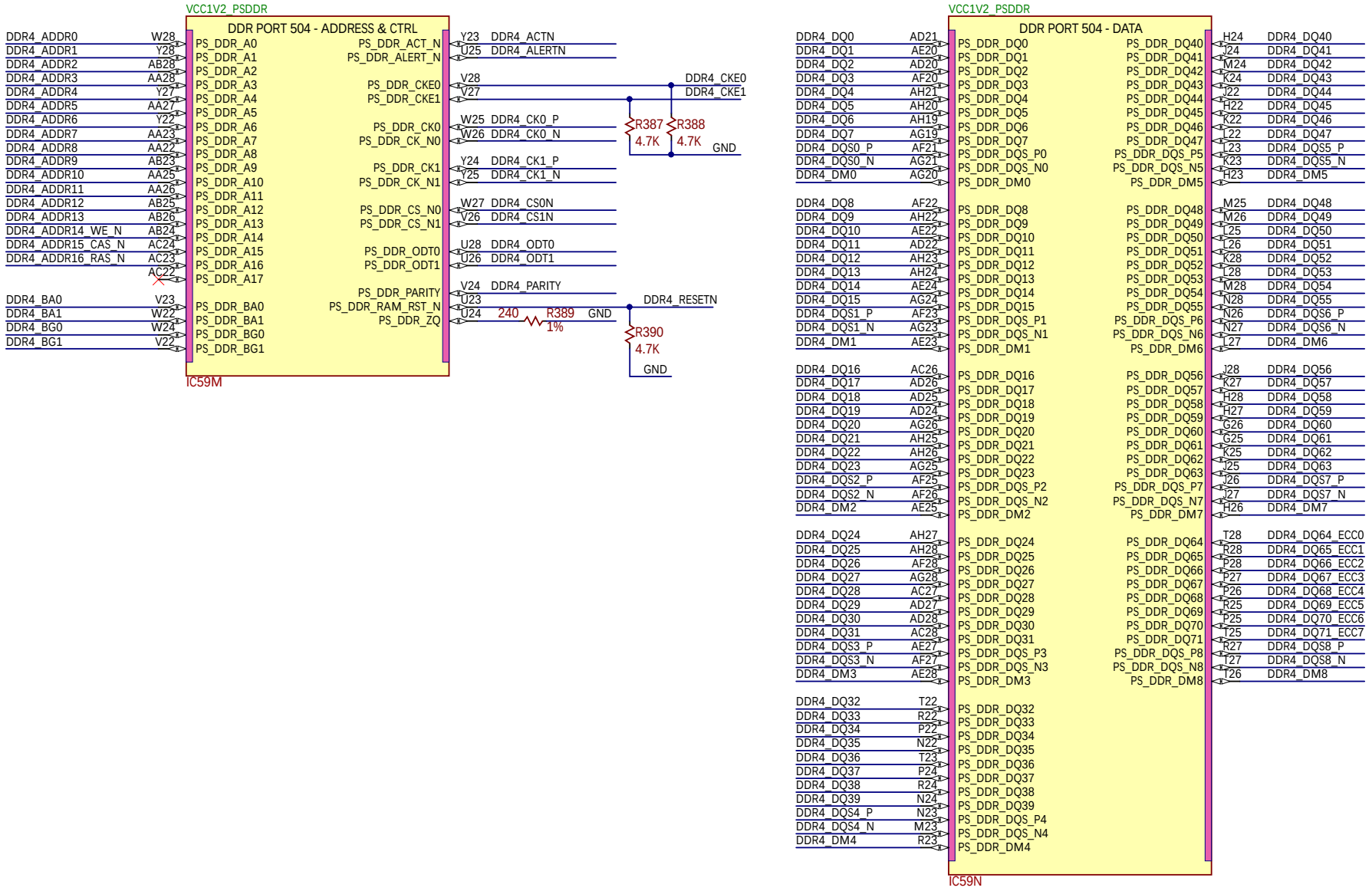
VCC1V2_PSDDR
DDR PORT 504 - ADDRESS & CTRL
DDR4_ADDR0 W28
DDR4_ADDR1 Y28
DDR4_ADDR2 AB28
DDR4_ADDR3 AA28
DDR4_ADDR4 Y27
DDR4_ADDR5 AA27
DDR4_ADDR6 Y22
DDR4_ADDR7 AA23
DDR4_ADDR8 AA22
DDR4_ADDR9 AB23
DDR4_ADDR10 AA25
DDR4_ADDR11 AA26
DDR4_ADDR12 AB25
DDR4_ADDR13 AB26
DDR4_ADDR14_WE_N AB24
DDR4_ADDR15_CAS_N AC24
DDR4_ADDR16_RAS_N AC23
AC22
DDR4_BA0 V23
DDR4_BA1 W22
DDR4_BG0 W24
DDR4_BG1 V22
PS_DDR_A0
PS_DDR_A1
PS_DDR_A2
PS_DDR_A3
PS_DDR_A4
PS_DDR_A5
PS_DDR_A6
PS_DDR_A7
PS_DDR_A8
PS_DDR_A9
PS_DDR_A10
PS_DDR_A11
PS_DDR_A12
PS_DDR_A13
PS_DDR_A14
PS_DDR_A15
PS_DDR_A16
PS_DDR_A17
PS_DDR_BA0
PS_DDR_BA1
PS_DDR_BG0
PS_DDR_BG1
PS_DDR_ACT_N
PS_DDR_ALERT_N
PS_DDR_CKE0
PS_DDR_CKE1
PS_DDR_CK0
PS_DDR_CK_N0
PS_DDR_CK1
PS_DDR_CK_N1
PS_DDR_CS_N0
PS_DDR_CS_N1
PS_DDR_ODT0
PS_DDR_ODT1
PS_DDR_PARITY
PS_DDR_RAM_RST_N
PS_DDR_ZQ
Y23 DDR4_ACTN
U25 DDR4_ALERTN
V28
V27
DDR4_CKE0
DDR4_CKE1
W25 DDR4_CK0_P
W26 DDR4_CK0_N
Y24 DDR4_CK1_P
Y25 DDR4_CK1_N
W27 DDR4_CS0N
V26 DDR4_CS1N
U28 DDR4_ODT0
U26 DDR4_ODT1
V24 DDR4_PARITY
U23
U24
240
R389
1%
GND
DDR4_RESETN
R387
4.7K
R388
4.7K
GND
R390
4.7K
GND
IC59M
VCC1V2_PSDDR
DDR PORT 504 - DATA
DDR4_DQ0 AD21
DDR4_DQ1 AE20
DDR4_DQ2 AD20
DDR4_DQ3 AF20
DDR4_DQ4 AH21
DDR4_DQ5 AH20
DDR4_DQ6 AH19
DDR4_DQ7 AG19
DDR4_DQS0_P AF21
DDR4_DQS0_N AG21
DDR4_DM0 AG20
DDR4_DQ8 AF22
DDR4_DQ9 AH22
DDR4_DQ10 AE22
DDR4_DQ11 AD22
DDR4_DQ12 AH23
DDR4_DQ13 AH24
DDR4_DQ14 AE24
DDR4_DQ15 AG24
DDR4_DQS1_P AF23
DDR4_DQS1_N AG23
DDR4_DM1 AE23
DDR4_DQ16 AC26
DDR4_DQ17 AD26
DDR4_DQ18 AD25
DDR4_DQ19 AD24
DDR4_DQ20 AG26
DDR4_DQ21 AH25
DDR4_DQ22 AH26
DDR4_DQ23 AG25
DDR4_DQS2_P AF25
DDR4_DQS2_N AF26
DDR4_DM2 AE25
DDR4_DQ24 AH27
DDR4_DQ25 AH28
DDR4_DQ26 AF28
DDR4_DQ27 AG28
DDR4_DQ28 AC27
DDR4_DQ29 AD27
DDR4_DQ30 AD28
DDR4_DQ31 AC28
DDR4_DQS3_P AE27
DDR4_DQS3_N AF27
DDR4_DM3 AE28
DDR4_DQ32 T22
DDR4_DQ33 R22
DDR4_DQ34 P22
DDR4_DQ35 N22
DDR4_DQ36 T23
DDR4_DQ37 P24
DDR4_DQ38 R24
DDR4_DQ39 N24
DDR4_DQS4_P N23
DDR4_DQS4_N M23
DDR4_DM4 R23
PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQS_P0
PS_DDR_DQS_N0
PS_DDR_DM0
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQS_P1
PS_DDR_DQS_N1
PS_DDR_DM1
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQS_P2
PS_DDR_DQS_N2
PS_DDR_DM2
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31
PS_DDR_DQS_P3
PS_DDR_DQS_N3
PS_DDR_DM3
PS_DDR_DQ32
PS_DDR_DQ33
PS_DDR_DQ34
PS_DDR_DQ35
PS_DDR_DQ36
PS_DDR_DQ37
PS_DDR_DQ38
PS_DDR_DQ39
PS_DDR_DQS_P4
PS_DDR_DQS_N4
PS_DDR_DM4
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PS_DDR_DQ41
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PS_DDR_DQ46
PS_DDR_DQ47
PS_DDR_DQS_P5
PS_DDR_DQS_N5
PS_DDR_DM5
PS_DDR_DQ48
PS_DDR_DQ49
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PS_DDR_DM7
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PS_DDR_DQ65
PS_DDR_DQ66
PS_DDR_DQ67
PS_DDR_DQ68
PS_DDR_DQ69
PS_DDR_DQ70
PS_DDR_DQ71
PS_DDR_DQS_P8
PS_DDR_DQS_N8
PS_DDR_DM8
H24 DDR4_DQ40
J24 DDR4_DQ41
M24 DDR4_DQ42
K24 DDR4_DQ43
J22 DDR4_DQ44
H22 DDR4_DQ45
K22 DDR4_DQ46
L22 DDR4_DQ47
L23 DDR4_DQS5_P
K23 DDR4_DQS5_N
H23 DDR4_DM5
M25 DDR4_DQ48
M26 DDR4_DQ49
L25 DDR4_DQ50
L26 DDR4_DQ51
K28 DDR4_DQ52
L28 DDR4_DQ53
M28 DDR4_DQ54
N28 DDR4_DQ55
N26 DDR4_DQS6_P
N27 DDR4_DQS6_N
L27 DDR4_DM6
J28 DDR4_DQ56
K27 DDR4_DQ57
H28 DDR4_DQ58
H27 DDR4_DQ59
G26 DDR4_DQ60
G25 DDR4_DQ61
K25 DDR4_DQ62
J25 DDR4_DQ63
J26 DDR4_DQS7_P
J27 DDR4_DQS7_N
H26 DDR4_DM7
T28 DDR4_DQ64_ECC0
R28 DDR4_DQ65_ECC1
P28 DDR4_DQ66_ECC2
P27 DDR4_DQ67_ECC3
P26 DDR4_DQ68_ECC4
R25 DDR4_DQ69_ECC5
P25 DDR4_DQ70_ECC6
T25 DDR4_DQ71_ECC7
R27 DDR4_DQS8_P
T27 DDR4_DQS8_N
T26 DDR4_DM8
IC59N
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
DDR BANK
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 26 out of 39
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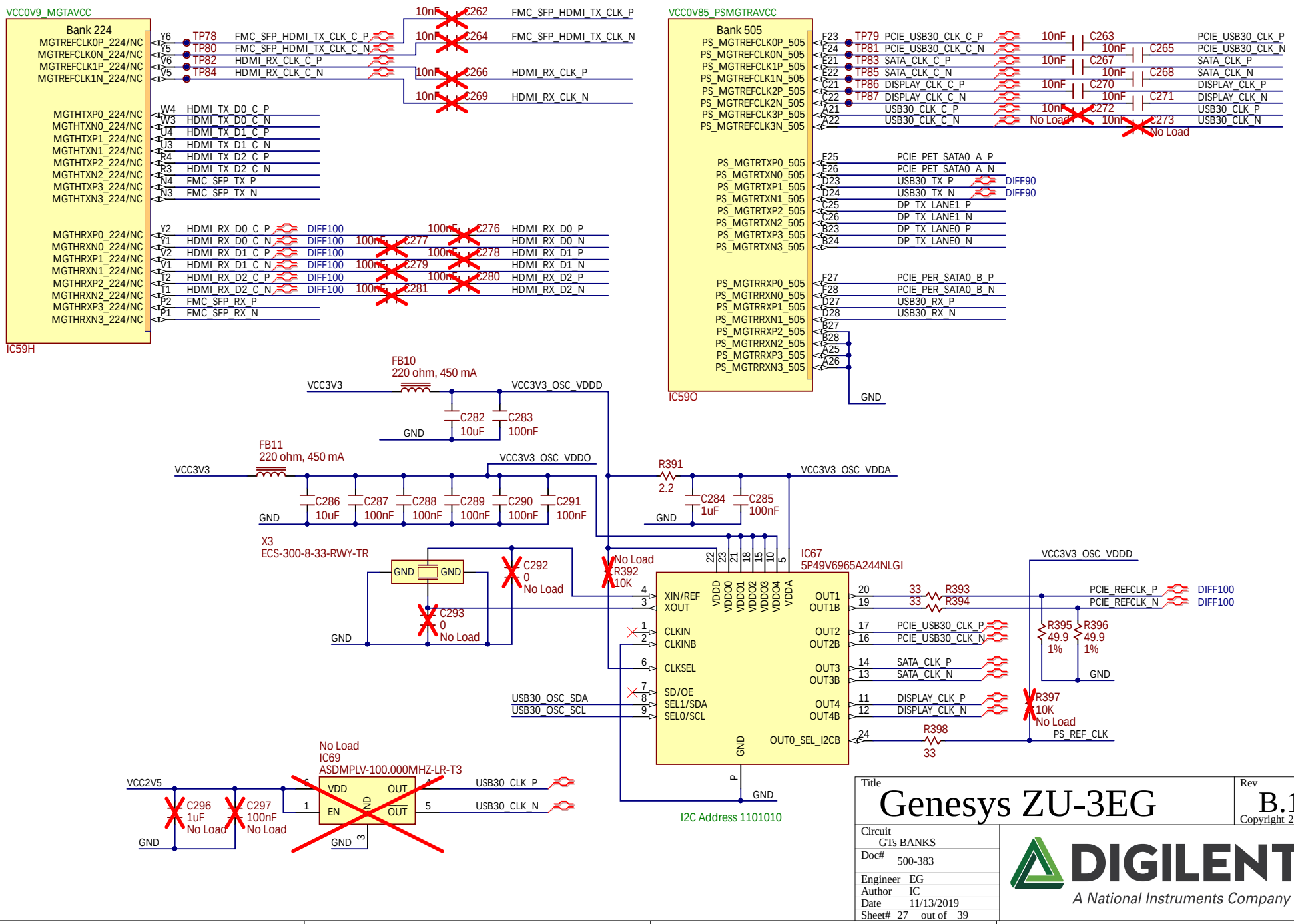
VCC0V9_MGTAVCC
Bank 224
IC59H
VCC0V85_PSMGTRAVCC
Bank 505
IC59O
FB10
220 ohm, 450 mA
FB11
220 ohm, 450 mA
X3
ECS-300-8-33-RWY-TR
IC67
5P49V6965A244NLGI
No Load
IC69
ASDMPLV-100.000MHZ-LR-T3
I2C Address 1101010
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
GTs BANKS
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 27 out of 39
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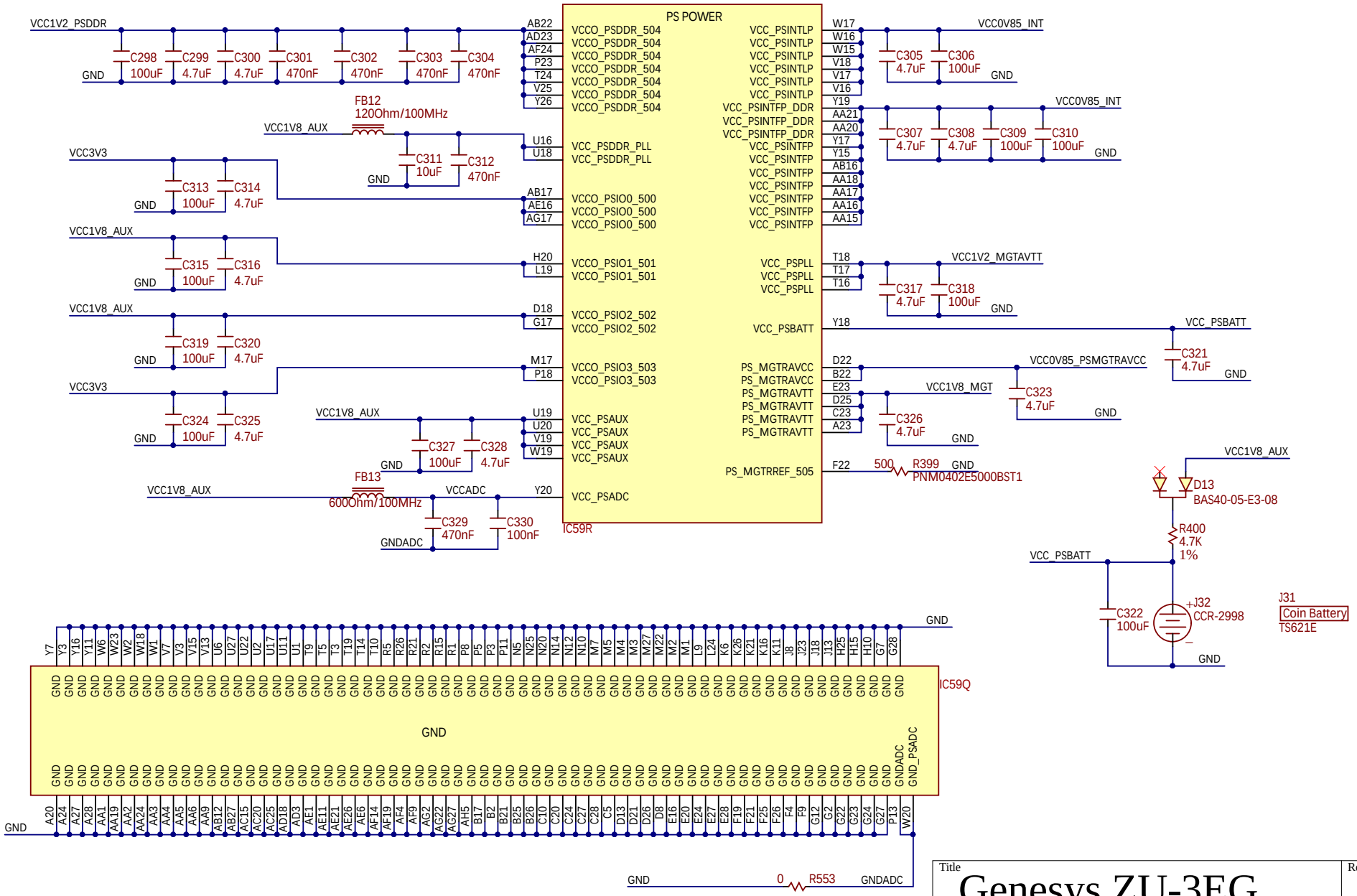
PS POWER
VCC1V2_PSDDR
C298 100uF
C299 4.7uF
C300 4.7uF
C301 470nF
C302 470nF
C303 470nF
C304 470nF
GND
AB22
AD23
AF24
P23
T24
V25
Y26
VCCO_PSDDR_504
FB12
120Ohm/100MHz
VCC1V8_AUX
C311 10uF
C312 470nF
U16
U18
VCC_PSDDR_PLL
VCC3V3
C313 100uF
C314 4.7uF
AB17
AE16
AG17
VCCO_PSIO0_500
H20
L19
VCCO_PSIO1_501
C315 100uF
C316 4.7uF
D18
G17
VCCO_PSIO2_502
C319 100uF
C320 4.7uF
M17
P18
VCCO_PSIO3_503
C324 100uF
C325 4.7uF
U19
U20
V19
W19
VCC_PSAUX
C327 100uF
C328 4.7uF
FB13
600Ohm/100MHz
VCCADC
Y20
VCC_PSADC
C329 470nF
C330 100nF
GNDADC
IC59R
W17
W16
W15
V18
V17
V16
VCC_PSINTLP
C305 4.7uF
C306 100uF
VCC0V85_INT
Y19
AA21
AA20
Y17
Y15
AB16
AA18
AA17
AA16
AA15
VCC_PSINTFP_DDR
VCC_PSINTFP
C307 4.7uF
C308 4.7uF
C309 100uF
C310 100uF
T18
T17
T16
VCC_PSPLL
C317 4.7uF
C318 100uF
VCC1V2_MGTAVTT
Y18
VCC_PSBATT
C321 4.7uF
D22
B22
E23
D25
C23
A23
PS_MGTRAVCC
PS_MGTRAVTT
VCC0V85_PSMGTRAVCC
C323 4.7uF
VCC1V8_MGT
C326 4.7uF
F22
PS_MGTRREF_505
500
R399
PNM0402E5000BST1
D13
BAS40-05-E3-08
R400 4.7K 1%
J32
CCR-2998
C322 100uF
J31
Coin Battery
TS621E
IC59Q
R553
0
GNDADC
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
PS POWER, GND
Doc#
500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 28 out of 39
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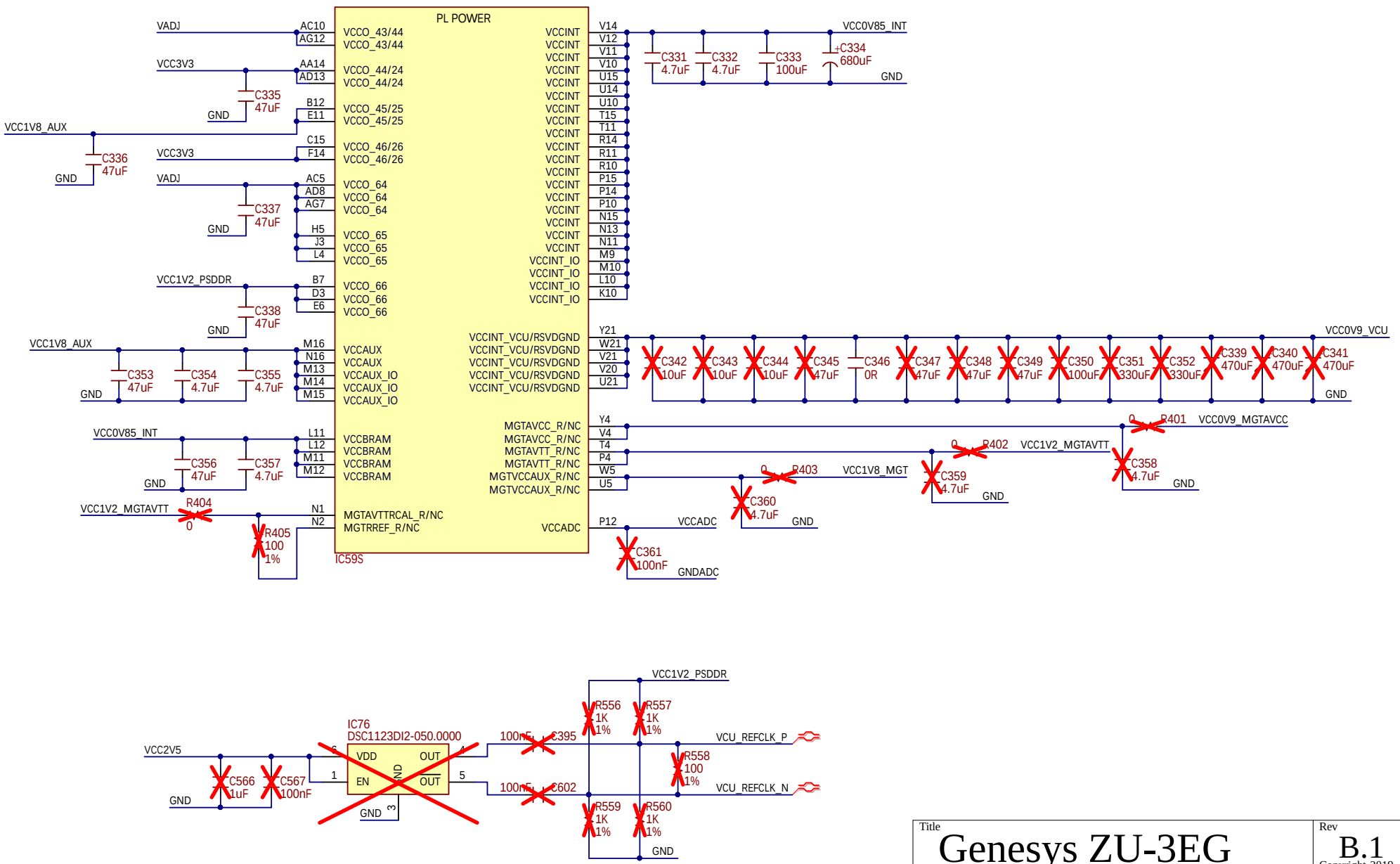

Title	Genesys ZU-3EG
Rev	B.1
Copyright	2019
Circuit	PL POWER; VCU OSC
Doc#	500-383
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Author	IC
Date	11/13/2019
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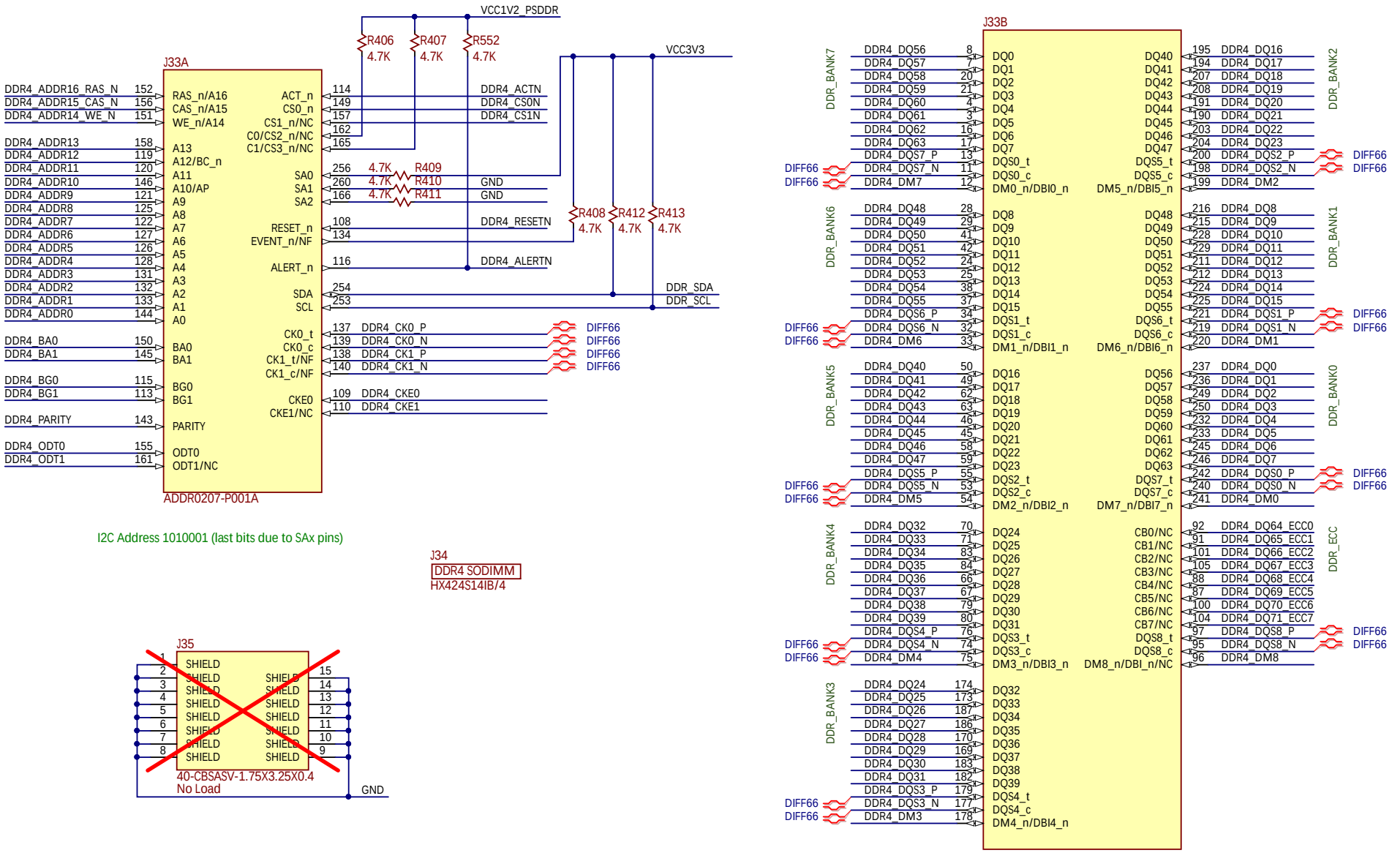
VCC1V2_PSDDR
R406 4.7K
R407 4.7K
R552 4.7K
VCC3V3
J33A
DDR4_ADDR16_RAS_N 152
DDR4_ADDR15_CAS_N 156
DDR4_ADDR14_WE_N 151
DDR4_ADDR13 158
DDR4_ADDR12 119
DDR4_ADDR11 120
DDR4_ADDR10 146
DDR4_ADDR9 121
DDR4_ADDR8 125
DDR4_ADDR7 122
DDR4_ADDR6 127
DDR4_ADDR5 126
DDR4_ADDR4 128
DDR4_ADDR3 131
DDR4_ADDR2 132
DDR4_ADDR1 133
DDR4_ADDR0 144
DDR4_BA0 150
DDR4_BA1 145
DDR4_BG0 115
DDR4_BG1 113
DDR4_PARITY 143
DDR4_ODT0 155
DDR4_ODT1 161
RAS_n/A16
CAS_n/A15
WE_n/A14
A13
A12/BC_n
A11
A10/AP
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BA0
BA1
BG0
BG1
PARITY
ODT0
ODT1/NC
ACT_n
CS0_n
CS1_n/NC
C0/CS2_n/NC
C1/CS3_n/NC
SA0
SA1
SA2
RESET_n
EVENT_n/NF
ALERT_n
SDA
SCL
CK0_t
CK0_c
CK1_t/NF
CK1_c/NF
CKE0
CKE1/NC
114 DDR4_ACTN
149 DDR4_CS0N
157 DDR4_CS1N
162
165
256 4.7K R409 GND
260 4.7K R410 GND
166 4.7K R411 GND
108 DDR4_RESETN
134
116 DDR4_ALERTN
254 DDR_SDA
253 DDR_SCL
137 DDR4_CK0_P
139 DDR4_CK0_N
138 DDR4_CK1_P
140 DDR4_CK1_N
109 DDR4_CKE0
110 DDR4_CKE1
R408 4.7K
R412 4.7K
R413 4.7K
DIFF66
ADDR0207-P001A
I2C Address 1010001 (last bits due to SAx pins)
J34
DDR4 SODIMM
HX424S14IB/4
J35
SHIELD
40-CBSASV-1.75X3.25X0.4
No Load
GND
J33B
DDR_BANK7
DDR_BANK6
DDR_BANK5
DDR_BANK4
DDR_BANK3
DDR_BANK2
DDR_BANK1
DDR_BANK0
DDR_ECC
DDR4_DQ56 8
DDR4_DQ57 7
DDR4_DQ58 20
DDR4_DQ59 21
DDR4_DQ60 4
DDR4_DQ61 3
DDR4_DQ62 16
DDR4_DQ63 17
DDR4_DQS7_P 13
DDR4_DQS7_N 11
DDR4_DM7 12
DDR4_DQ48 28
DDR4_DQ49 29
DDR4_DQ50 41
DDR4_DQ51 42
DDR4_DQ52 24
DDR4_DQ53 25
DDR4_DQ54 38
DDR4_DQ55 37
DDR4_DQS6_P 34
DDR4_DQS6_N 32
DDR4_DM6 33
DDR4_DQ40 50
DDR4_DQ41 49
DDR4_DQ42 62
DDR4_DQ43 63
DDR4_DQ44 46
DDR4_DQ45 45
DDR4_DQ46 58
DDR4_DQ47 59
DDR4_DQS5_P 55
DDR4_DQS5_N 53
DDR4_DM5 54
DDR4_DQ32 70
DDR4_DQ33 71
DDR4_DQ34 83
DDR4_DQ35 84
DDR4_DQ36 66
DDR4_DQ37 67
DDR4_DQ38 79
DDR4_DQ39 80
DDR4_DQS4_P 76
DDR4_DQS4_N 74
DDR4_DM4 75
DDR4_DQ24 174
DDR4_DQ25 173
DDR4_DQ26 187
DDR4_DQ27 186
DDR4_DQ28 170
DDR4_DQ29 169
DDR4_DQ30 183
DDR4_DQ31 182
DDR4_DQS3_P 179
DDR4_DQS3_N 177
DDR4_DM3 178
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
DQS0_t DQS0_c DM0_n/DBI0_n
DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
DQS1_t DQS1_c DM1_n/DBI1_n
DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23
DQS2_t DQS2_c DM2_n/DBI2_n
DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
DQS3_t DQS3_c DM3_n/DBI3_n
DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39
DQS4_t DQS4_c DM4_n/DBI4_n
DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47
DQS5_t DQS5_c DM5_n/DBI5_n
DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55
DQS6_t DQS6_c DM6_n/DBI6_n
DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
DQS7_t DQS7_c DM7_n/DBI7_n
CB0/NC CB1/NC CB2/NC CB3/NC CB4/NC CB5/NC CB6/NC CB7/NC
DQS8_t DQS8_c DM8_n/DBI_n/NC
195 DDR4_DQ16
194 DDR4_DQ17
207 DDR4_DQ18
208 DDR4_DQ19
191 DDR4_DQ20
190 DDR4_DQ21
203 DDR4_DQ22
204 DDR4_DQ23
200 DDR4_DQS2_P
198 DDR4_DQS2_N
199 DDR4_DM2
216 DDR4_DQ8
215 DDR4_DQ9
228 DDR4_DQ10
229 DDR4_DQ11
211 DDR4_DQ12
212 DDR4_DQ13
224 DDR4_DQ14
225 DDR4_DQ15
221 DDR4_DQS1_P
219 DDR4_DQS1_N
220 DDR4_DM1
237 DDR4_DQ0
236 DDR4_DQ1
249 DDR4_DQ2
250 DDR4_DQ3
232 DDR4_DQ4
233 DDR4_DQ5
245 DDR4_DQ6
246 DDR4_DQ7
242 DDR4_DQS0_P
240 DDR4_DQS0_N
241 DDR4_DM0
92 DDR4_DQ64_ECC0
91 DDR4_DQ65_ECC1
101 DDR4_DQ66_ECC2
105 DDR4_DQ67_ECC3
88 DDR4_DQ68_ECC4
87 DDR4_DQ69_ECC5
100 DDR4_DQ70_ECC6
104 DDR4_DQ71_ECC7
97 DDR4_DQS8_P
95 DDR4_DQS8_N
96 DDR4_DM8
Title
Genesys ZU-3EG
Rev
B.1
Copyright 2019
Circuit
DDR4 SODIMM INTFC
Doc# 500-383
Engineer EG
Author IC
Date 11/13/2019
Sheet# 30 out of 39
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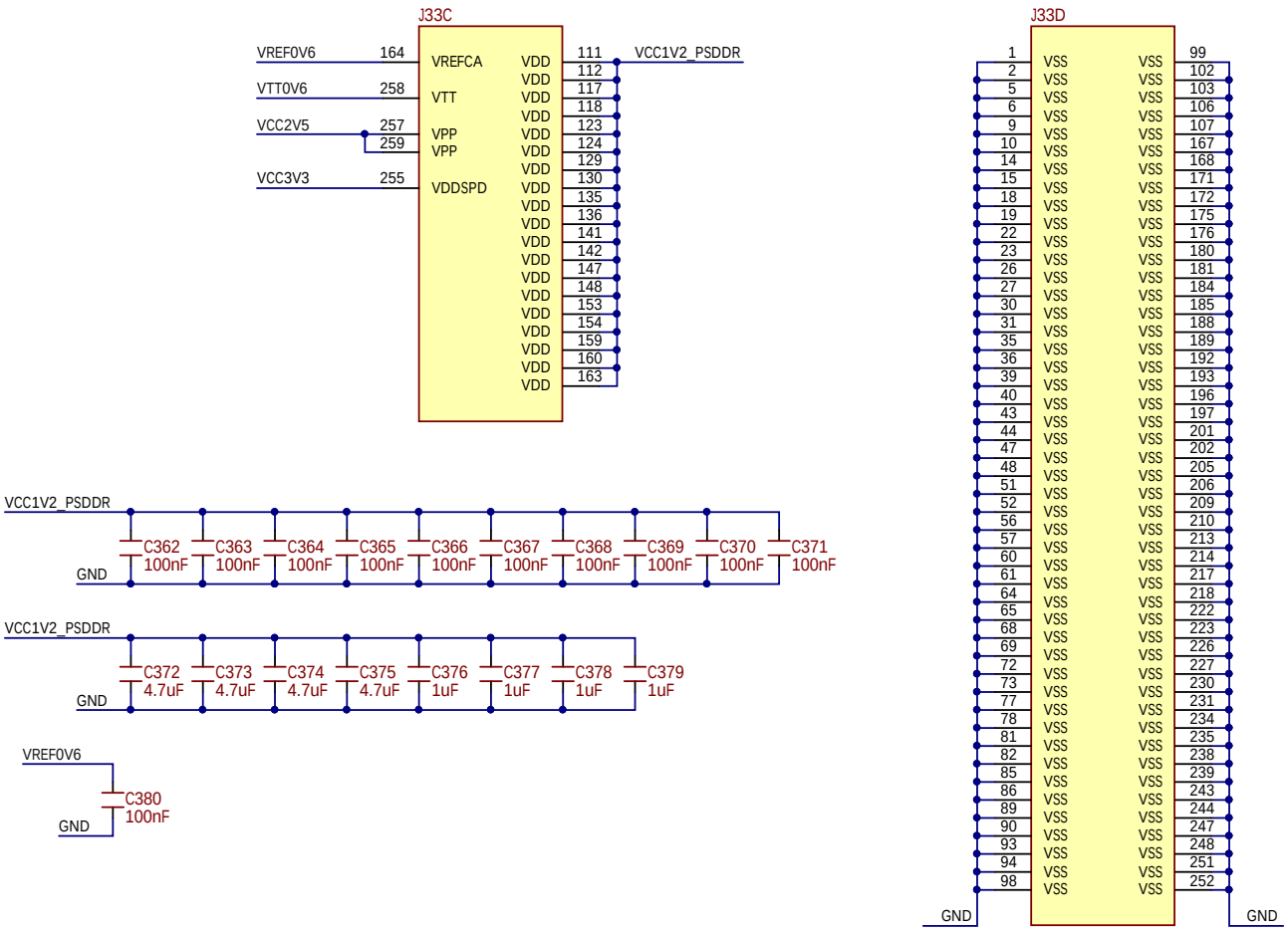

Title	Genesys ZU-3EG
Rev	B.1
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Circuit	DDR4 SODIMM SUPPLIES
Doc#	500-383
Engineer	EG
Author	IC
Date	11/13/2019
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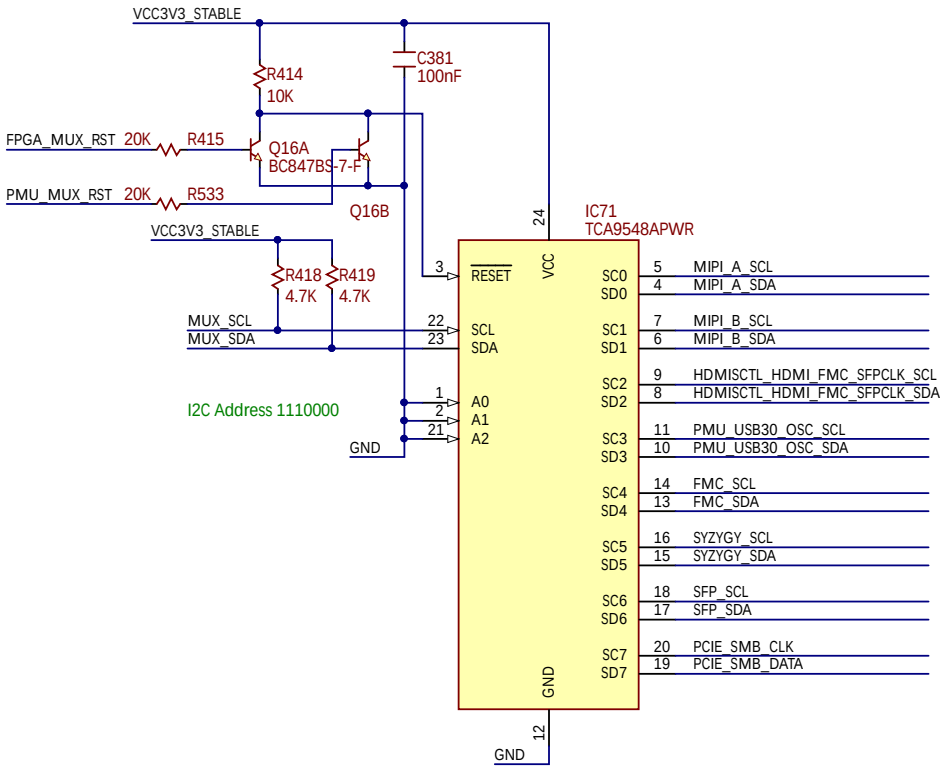

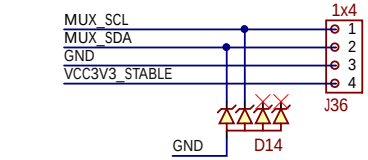

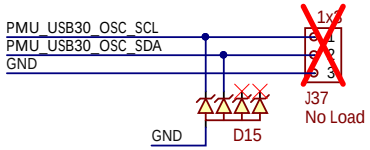

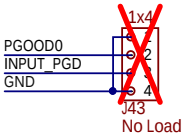

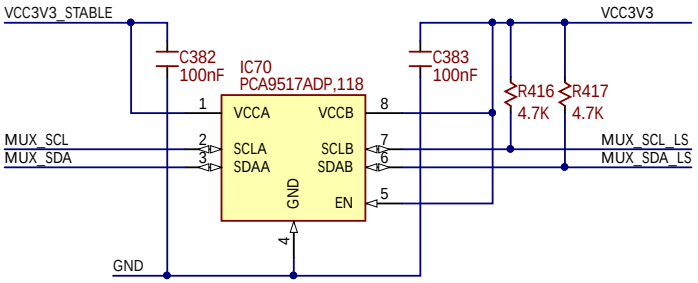

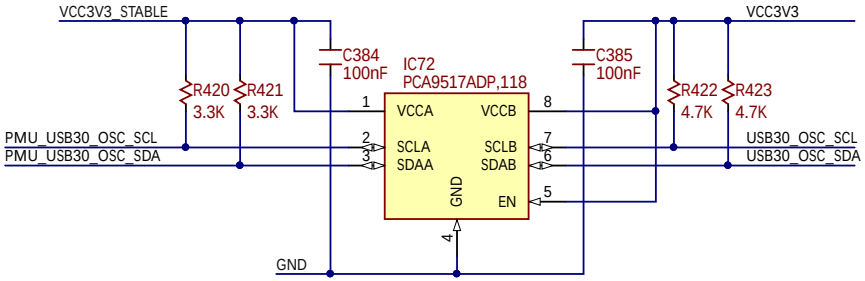

Title	Genesys ZU-3EG
Rev	B.1
Copyright	2019
Circuit	I2C Interfaces
Doc#	500-383
Engineer	EG
Author	IC
Date	11/13/2019
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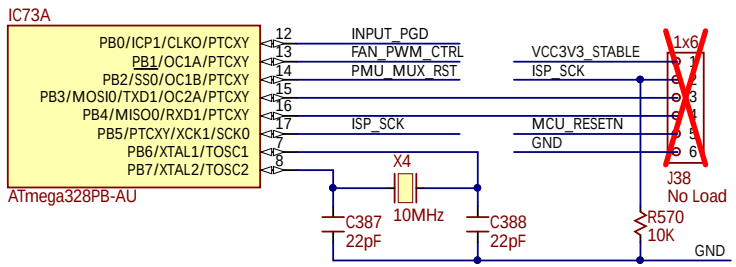

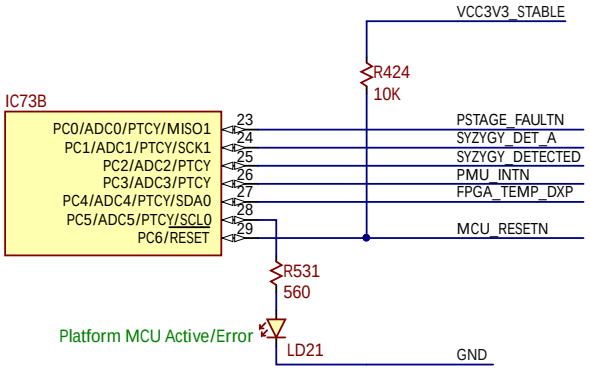

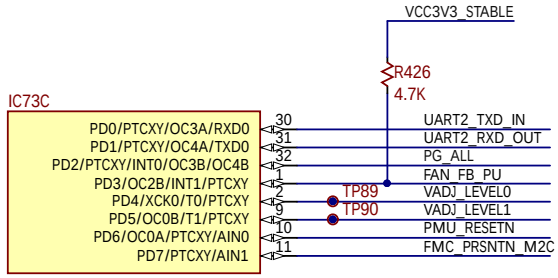

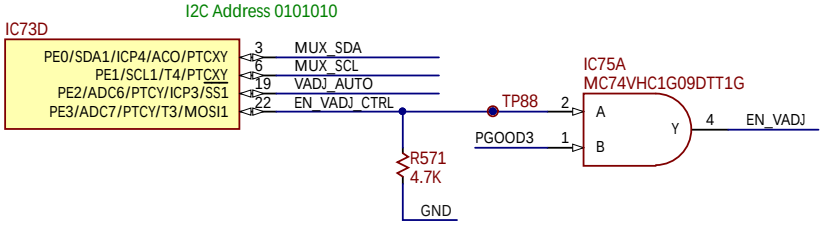

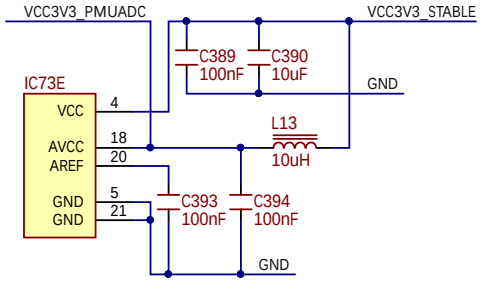

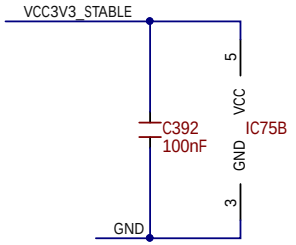

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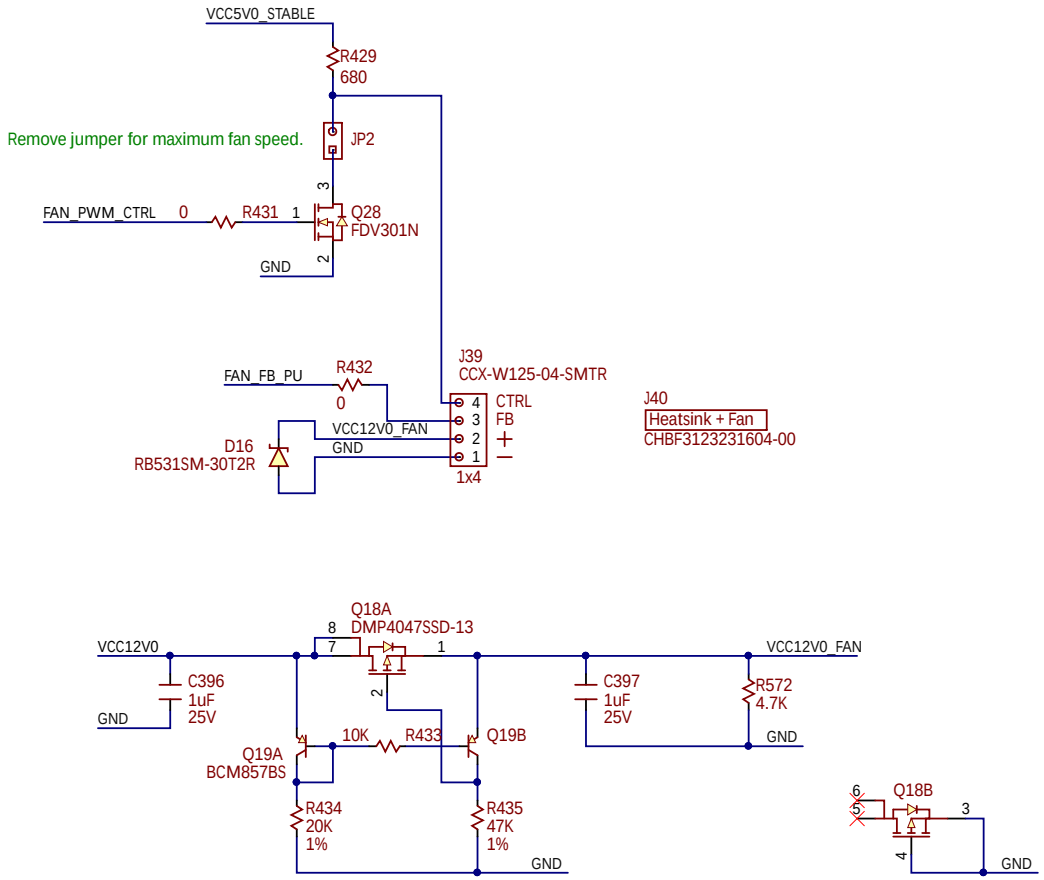

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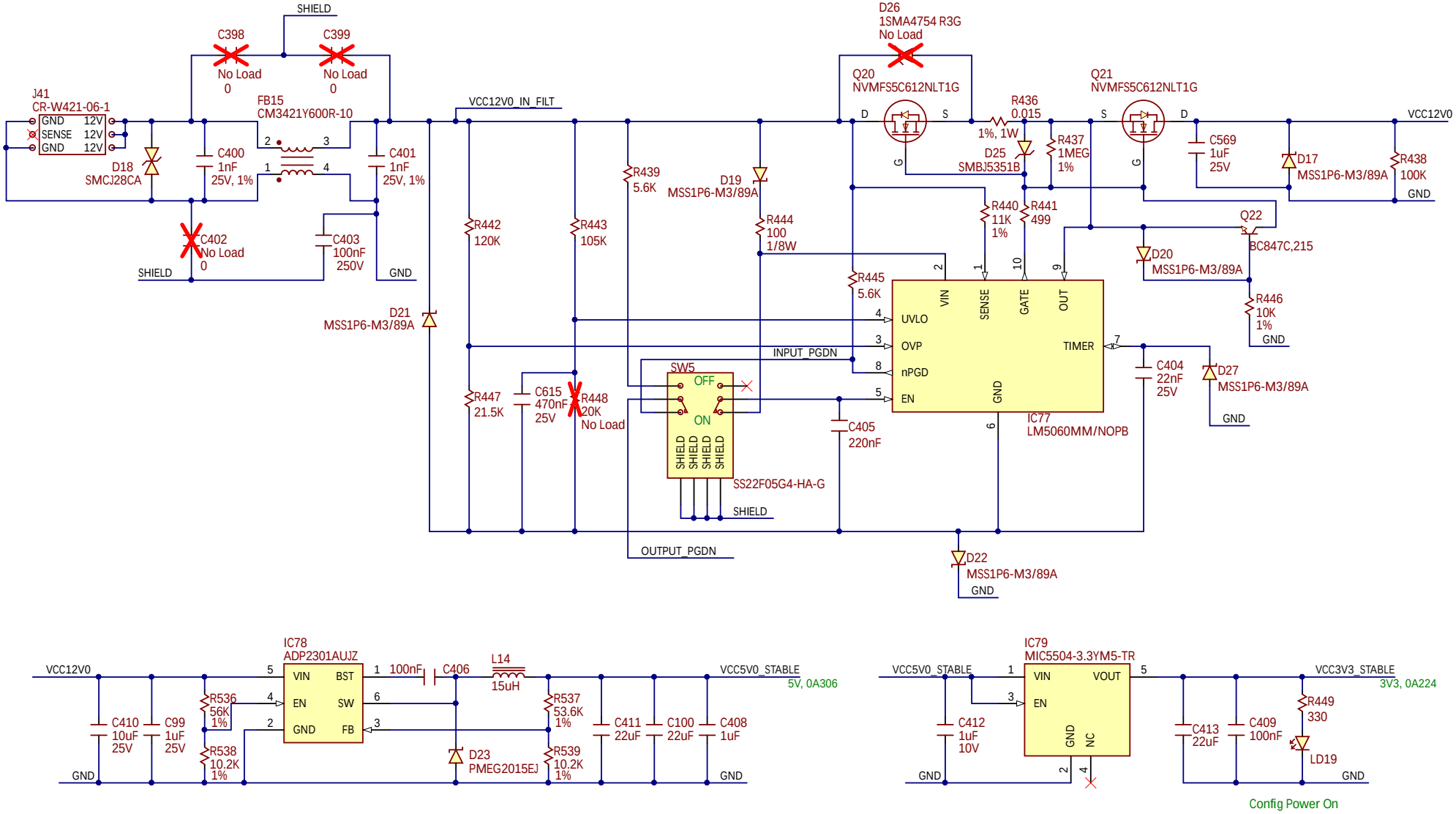

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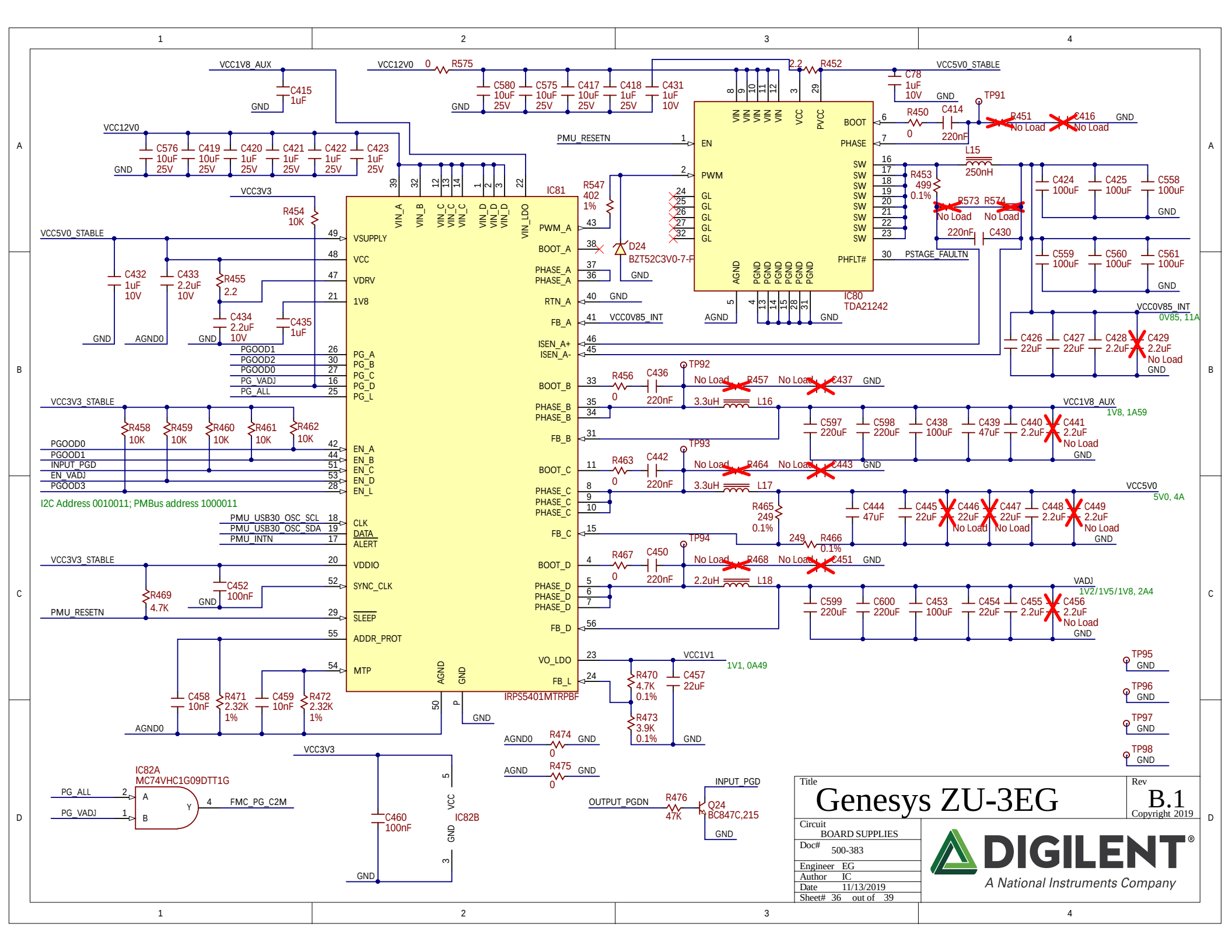
VCC1V8_AUX
VCC12V0
VCC5V0_STABLE
VCC3V3
VCC3V3_STABLE
IC81
IRPS5401MTRPBF
IC80
TDA21242
IC82A
MC74VHC1G09DTT1G
IC82B
D24
BZT52C3V0-7-F
L15
250nH
L16
3.3uH
L17
3.3uH
L18
2.2uH
PMU_RESETN
PSTAGE_FAULTN
VCC0V85_INT
0V85, 11A
VCC1V8_AUX
1V8, 1A59
VCC5V0
5V0, 4A
VADJ
1V2/1V5/1V8, 2A4
VCC1V1
1V1, 0A49
PGOOD0
PGOOD1
INPUT_PGD
EN_VADJ
PGOOD3
I2C Address 0010011; PMBus address 1000011
PMU_USB30_OSC_SCL
PMU_USB30_OSC_SDA
PMU_INTN
PG_ALL
PG_VADJ
FMC_PG_C2M
OUTPUT_PGDN
Q24
BC847C,215
TP91
TP92
TP93
TP94
TP95
TP96
TP97
TP98
No Load
GND
AGND
AGND0
Title
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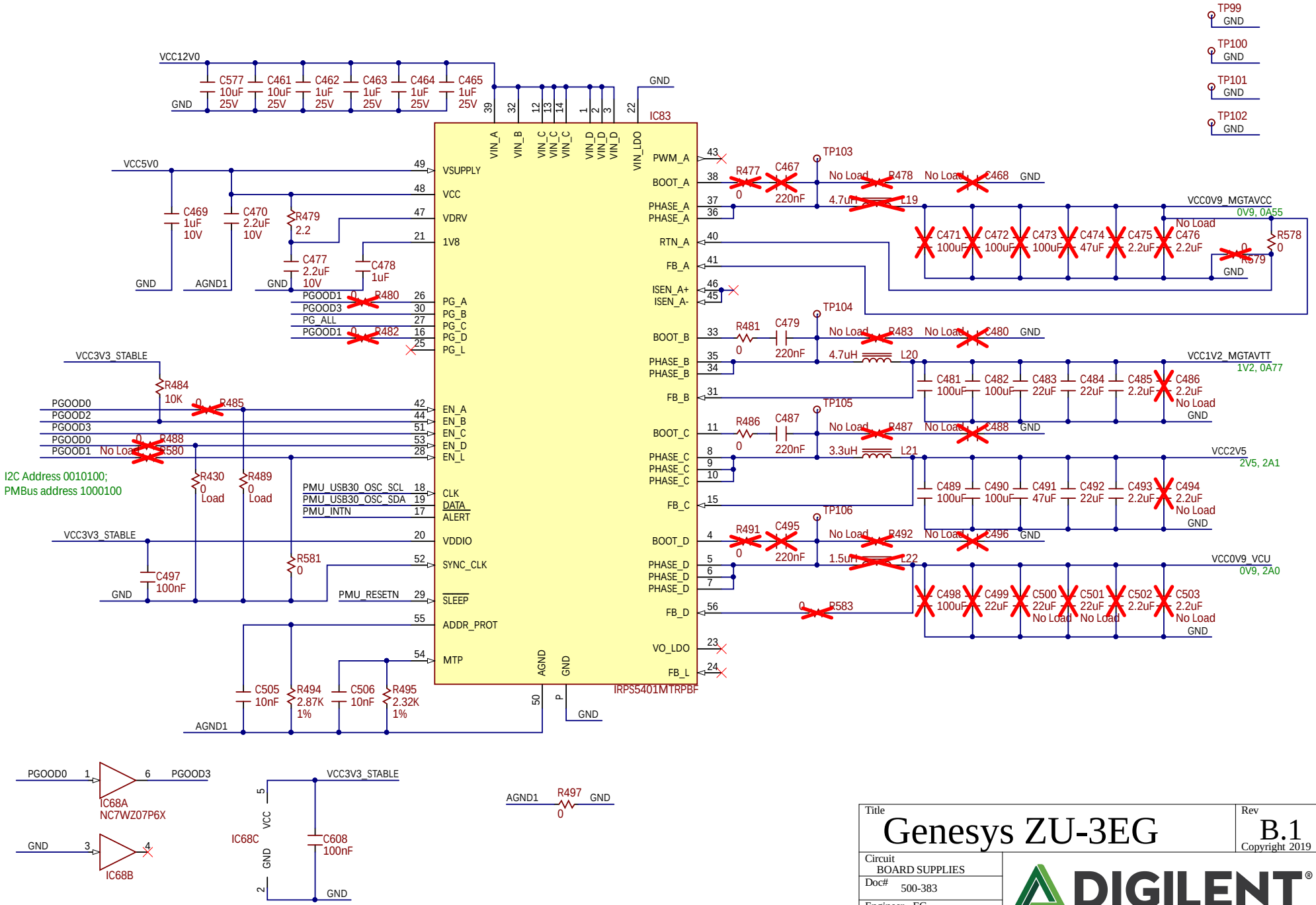

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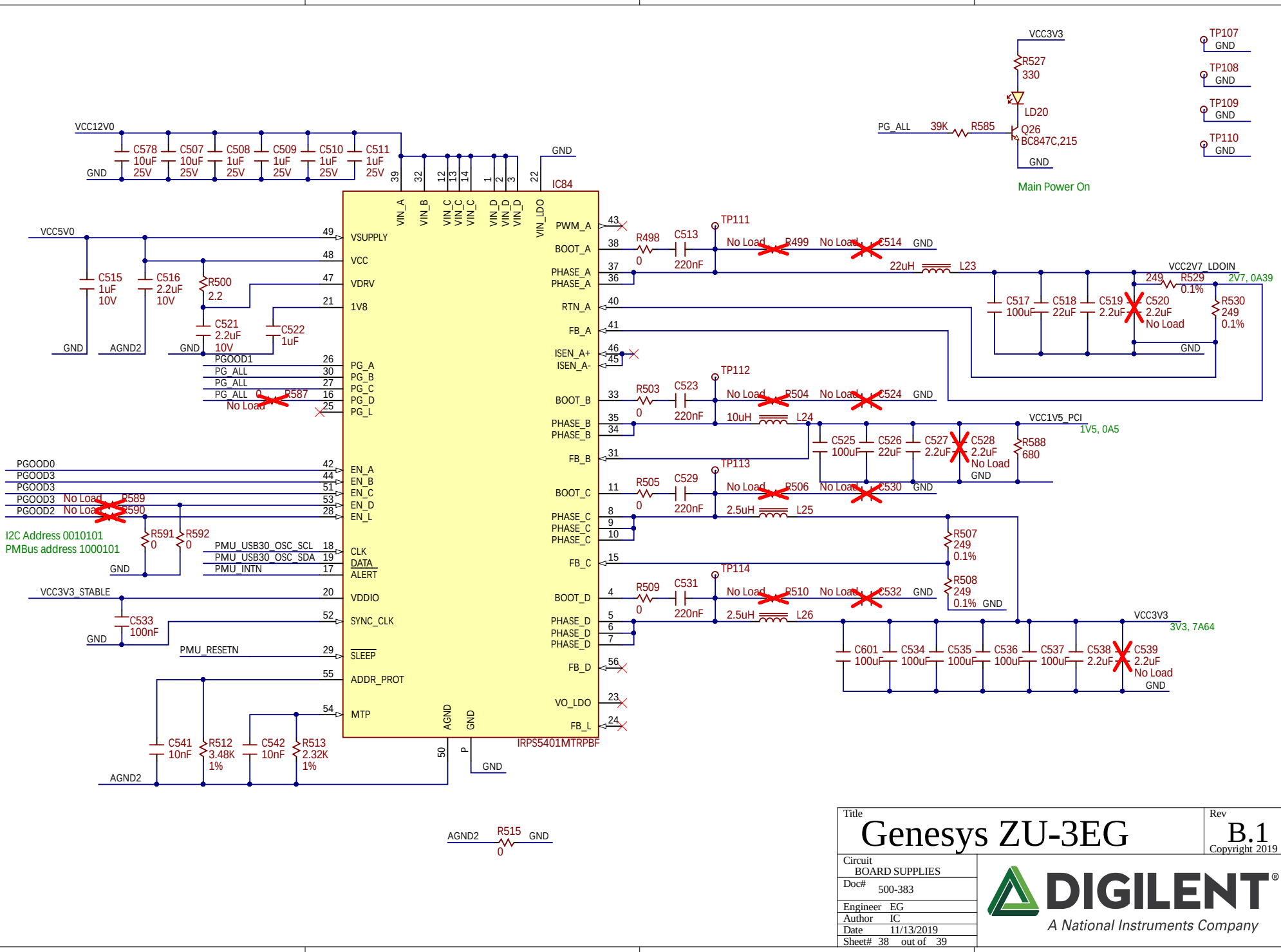

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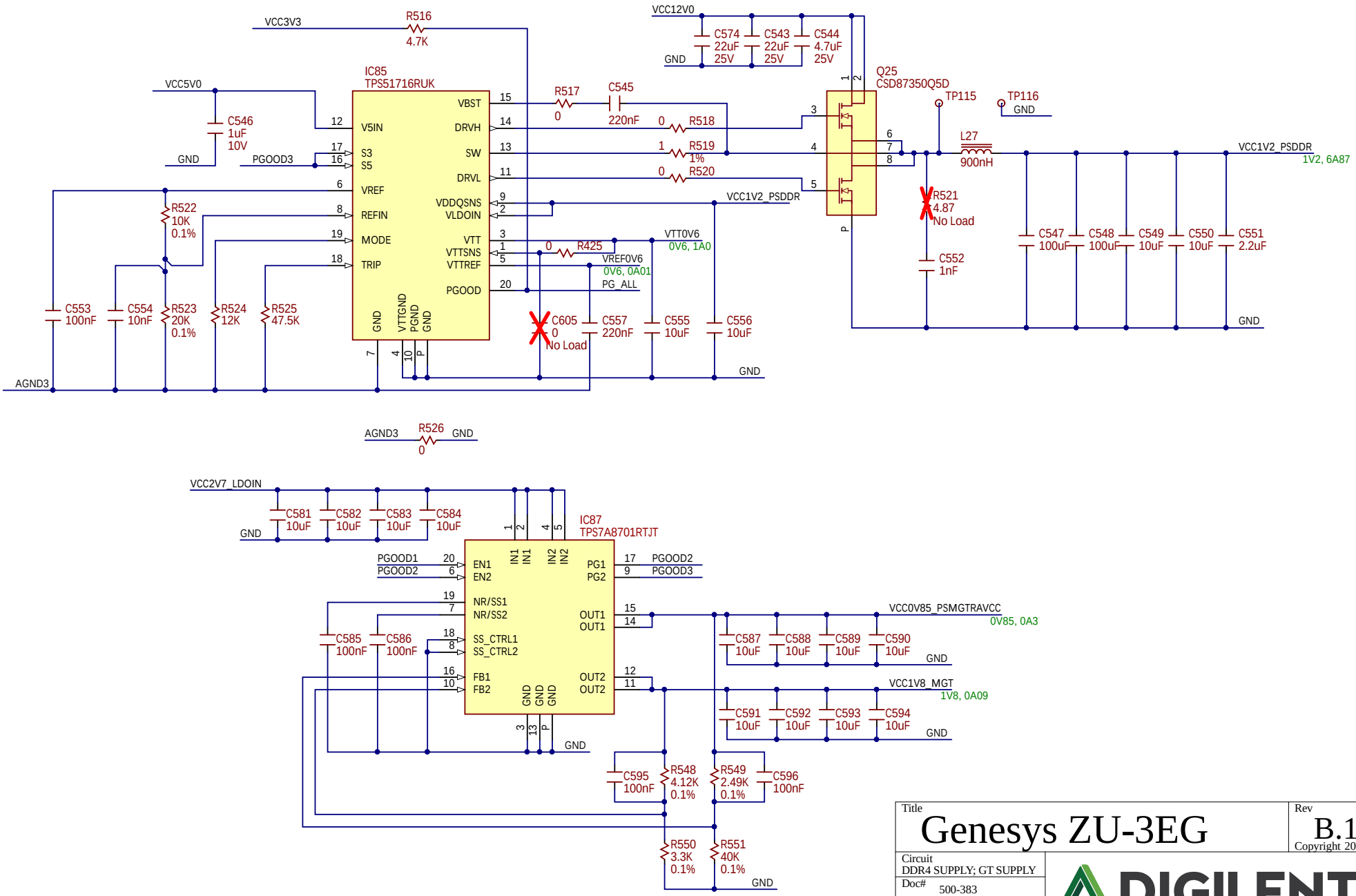

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