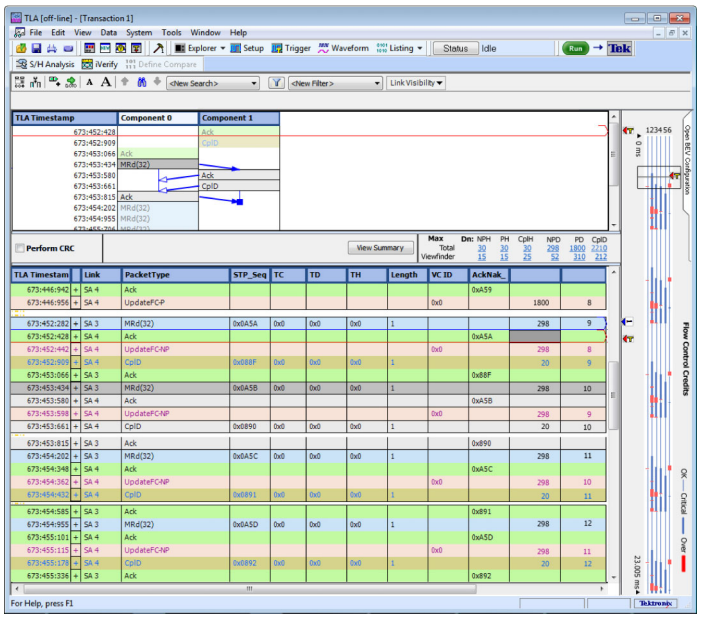
Tektronix PCI Express Logic Protocol Analyzer

TLA7SA00 Series Data Sheet



Features & Benefits

- PCI Express Gen1, Gen2, and Gen3 Protocol to Physical Layer Analysis for Link Widths from x1 through x16 with up to 8.0 GT/s Acquisition Rates
- Comprehensive PCI Express Probing Solutions, including Midbus, Slot Interposer, and Solder-down Probes
  - Nonintrusive Probing that Utilizes OpenEYE Technology incorporating Automatic Tuning Equalization Circuitry to allow Probing Anywhere on the Channel and Ensure Accurate Data Capture in PCI Express Systems with Channel Lengths up to 24 in. and 2 Connectors
  - Single-click Calibration Process Calibrates the Analyzer and Probes to the Target BER, Calibration Results for Analyzer/Probe Sets are Remembered from One Session to Another
  - ScopePHY provides the ability to Quickly Connect Any of the PCI Express Midbus, Slot Interposer, or Solder-down Probes to a High-performance Oscilloscope providing a More Detailed Analog View of the PHY Layer
- Shorten Time to Gain Confidence in the Test System Setup
  - Front-panel LEDs provide Status Information such as Link Speed, Symbol Lock, and Link Activity
  - Auto-configure sets up the Logic Protocol Analyzer System to be Ready for Data Acquisition Quickly
  - FastSYNC Tracks the Link as it Transitions In and Out of ASPM Power States such as L0s, Regardless of Electrical Idle Duration
  - Real-time Statistics Help Observe Link Health and Behavior over Time
- Powerful Trigger-state Machine Spans All Layers of the Protocol
  - 8 States
  - 8 Packet Recognizers
  - 4 Symbol Sequence Recognizers
  - 4 Counter/Timers
  - 4 Event Flags
  - Conditional Storage
  - Real-time Filtering
- Industry's Deepest 8 GB Memory/Module (16 GB memory, x16 link width) Increases the Chances of Capturing an Error and the Fault that Caused the Error
- HW Accelerated Search and Data Displays provide Immediate Visibility of Data Regardless of Record Length
- Information Density for Rapid Data Analysis
  - The Transaction Window provides Visibility into Protocol Behavior at the Packet and Transaction Level interspersed with Physical Layer Activity
  - Innovative Bird's Eye View provides a High-ground Visibility of System Issues involving Flow Control
  - The Summary Profile Window Helps Ascertain the Health of the System and Identify Patterns of Interest such as Errors, TLPs, DLLPs, Ordered Sets, etc.
- Multibus Visibility for System-level Debug
  - Analyze Complete System Interactions with Time-correlated, Multibus Analysis on a Single Display on a Single Mainframe. For example, Tracing Memory Access from PCI Express to DDR Memory or Monitor Multiple PCIe Links on a PCIe Switch
  - Cross Triggering and a Common Global Time Stamp enables Accurate and Efficient Debugging by Showing Exactly What Was Happening on One Bus Relative to Another at Any Given Instant in Time

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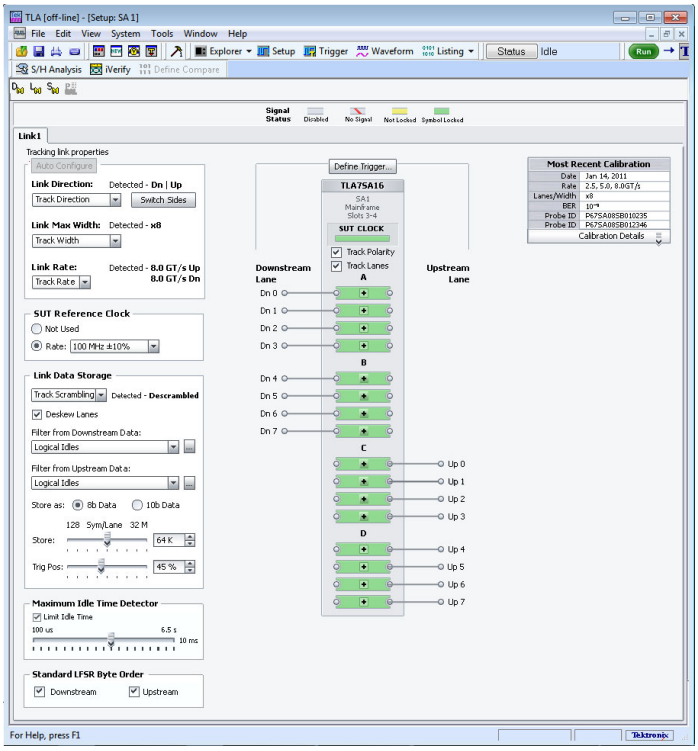
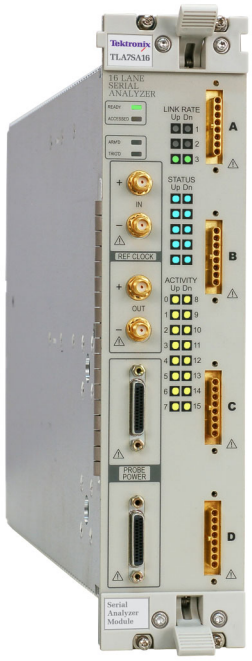


The TLA7SA00 Series Logic Protocol Analyzer Setup window provides a quick overview of link connection status.



TLA7SA16 Logic Protocol Analyzer Module.

Applications

- PCI Express Debug from Protocol Layer to Physical Layer
  - Silicon Validation
  - Computer System Validation
  - Embedded System Debug and Validation
- Processor/Bus Debug and Verification
- Embedded Software Integration, Debug, and Verification

PCI Express Debug and Analysis spanning Physical- to Transaction-layer with Feature-rich Hardware

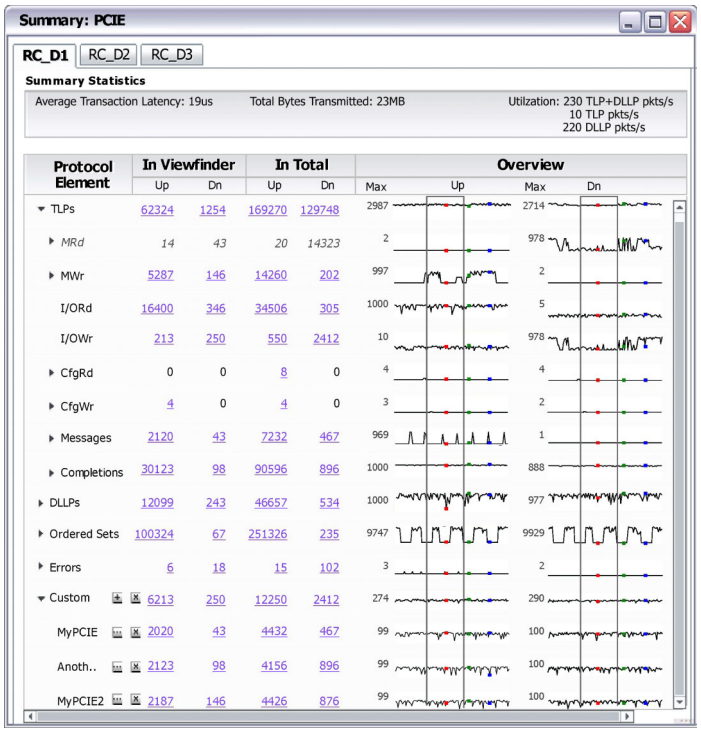
PCI Express 3.0 introduces new challenges for validation engineers. Time-to-market pressures require a solution that can quickly pinpoint problems. The TLA7SA00 Series logic protocol analyzer modules provide an innovative approach to PCI Express validation that spans all layers of the protocol from the physical layer to the transaction layer.

Reduce the time to information by viewing and searching up to 16 GB deep memory in just seconds with rapid display updates enabled by our industry-leading hardware acceleration.

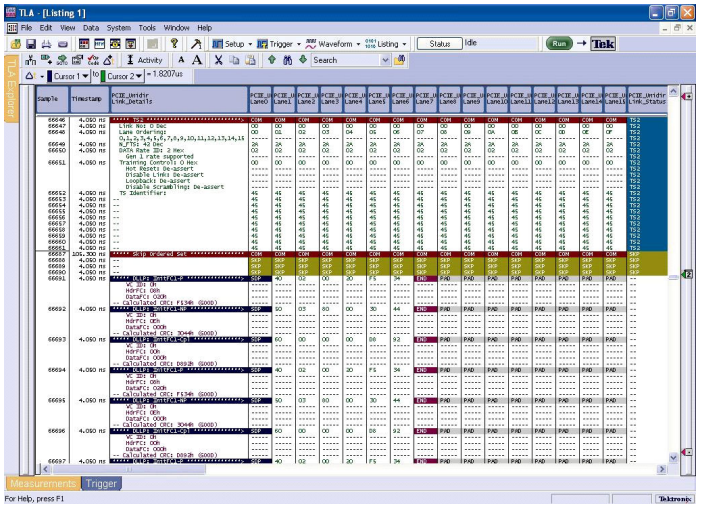
Features such as auto-training, auto-tracking, front-panel LED lane status, single-click calibration, etc. allow the logic protocol analyzer to "wire" itself automatically which shortens the time it takes for users to build confidence in the test system.

Quickly trigger on patterns of interest with powerful trigger capabilities that span across all protocol layers. Real-time filtering provides the ability to filter unwanted data and use the acquisition memory more efficiently by storing only transactions of interest.

Elusive power state anomalies pertaining to entry into and exit from electrical idle and ASPM states such as L0s to L0 are easily addressed by FastSYNC technology. It ensures quick re-synchronization of the logic protocol analyzer with the PCI Express FTS ordered sets regardless of the duration of Electrical Idle time. This capability is unique compared to other solutions where the L0s to L0 re-synchronization time is specified only over a short Electrical Idle time of 2 µs or less.



Summary Profile window.



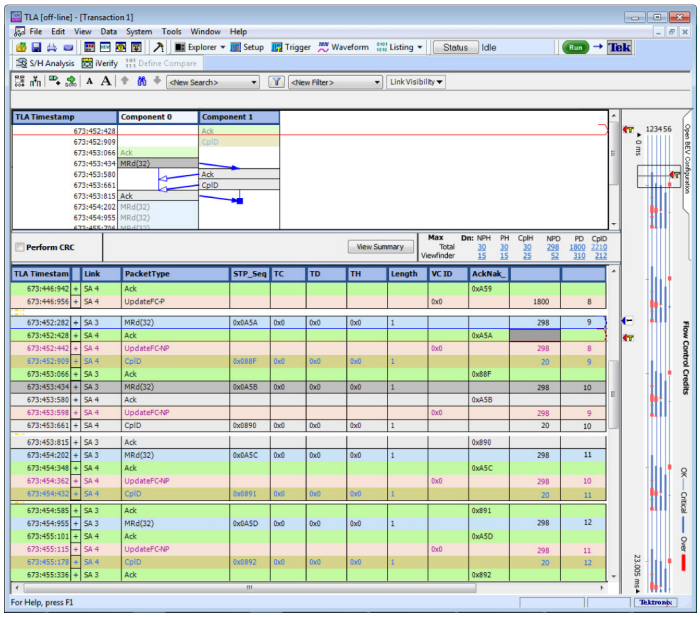
Listing window showing packet details as well as lane-by-lane symbol decode.

Innovative Data Displays for Accelerated Time to Information

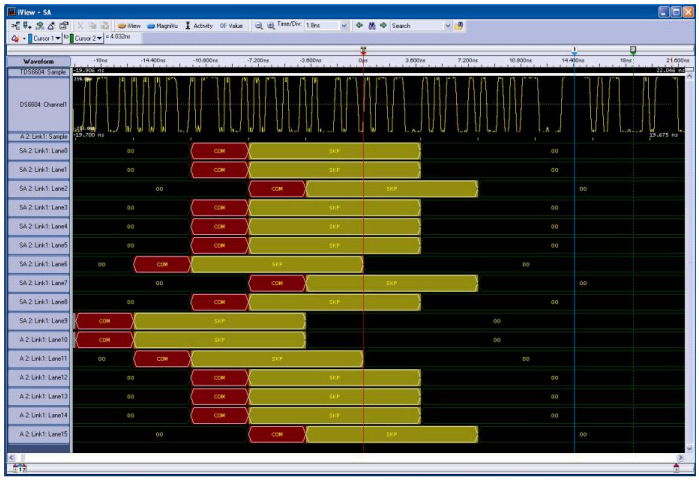
The new PCI Express software helps view information in a hierarchical and rich format. Protocol information can be expanded and collapsed to rapidly display or hide information as needed.

Quickly ascertain the health of the system and identify patterns of interest (errors, specific transactions, ordered sets, etc.) with statistical summary and data graphs using the Summary Profile window. Summary statistics include useful information such as average transaction latency, total bytes transmitted, and bus utilization.

Protocol behavior can be viewed at the packet and transaction level interspersed with physical layer activity in a single innovative Transaction



Transaction window with integrated Bird's Eye View.

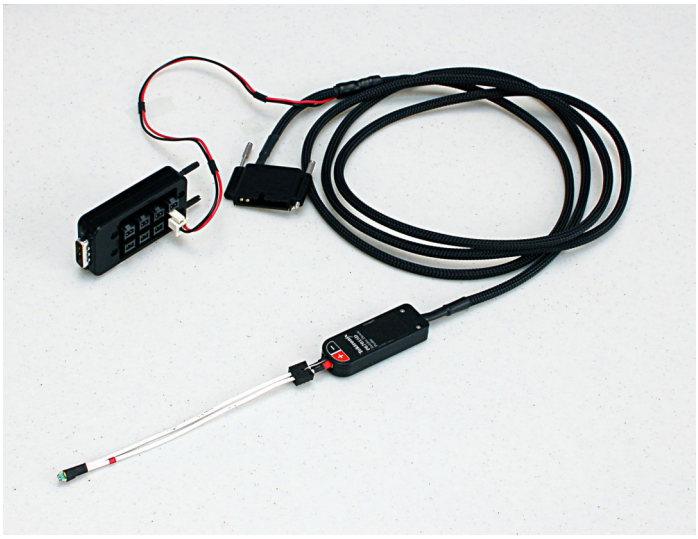


Waveform window showing individual lane activity correlated with analog waveform.

window. The Transaction Stitching feature shows packets participating in a completed transaction or incomplete transactions as errors in a diagrammatic representation. Additional capabilities, including color coding of the packets, cursor locking across multiple data windows, and a unique Bird's Eye View integrated with the Transaction window provides a high-ground visibility of system issues involving flow control.

Further insight into physical layer details can be gained with the unique Listing window showing packet details as well as lane-by-lane symbol decode. You can also view individual lane activity correlated with analog waveforms from your high-bandwidth oscilloscope in the Waveform window.

Hardware developers, hardware/software integrators, and embedded system designers will appreciate the tight integration with the Tektronix Logic Analyzer. This provides visibility of complete system interactions with time-correlated, multibus analysis on a single display. Cross triggering and a common global time stamp enables accurate and efficient debugging by showing exactly what was happening on one bus relative to another at any given instant of time.

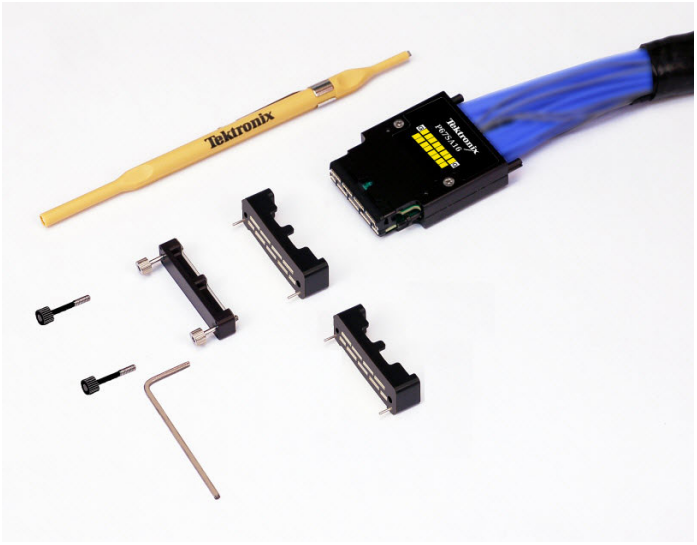


P67SA01SD – Single Differential Input PCI Express Solder-down Probe, shown with Option 1P power adapter.

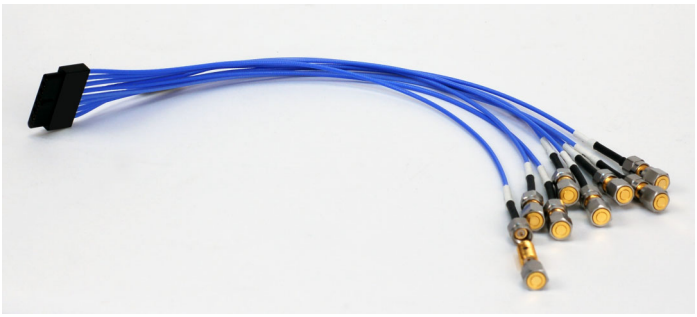
P67SA16S – x16 PCI Express Slot Interposer Probe. (x8, x4, x1 slot interposer probes also available)

High-performance PCI Express Probing Solutions for Different Application Needs

The P67SA00 Series probes provide validation engineers with a comprehensive set of PCI Express probing solutions, including midbus, slot interposer, and solder-down connectors. With support for PCI Express Gen1, Gen2, and Gen3 channel lengths up to 24 in. with 2 connectors,



P67SA16 – x8 PCI Express Midbus Probe and Accessories. (x4 midbus probe also available)



P67UHDSMA – x2 PCI Express Probe Lead Set for P67SA00 probe connections to oscilloscopes.

these probes utilize OpenEYE technology offering minimal electrical loading with the highest signal fidelity and active equalization to ensure accurate data recovery of closed eyes. All P67SA00 Series probes feature a graphical lane-swizzling capability for maximum flexibility to accommodate unique circuit board layouts.

With ScopePHY, quickly connect any of the probe connector outputs to an oscilloscope using the P67UHDSMA probe lead set to gain further insight into the PHY layer. Tektronix-supplied S-parameters of the probe and module configure a Tektronix oscilloscope's DSP filters to show the PCI Express link data eye at the probe tip.

Characteristics

TLA7SA00 Series

General

Characteristic	Description
Acquisition Rate with Frequency Margin	8 GT/s (+5% to –10%) 5 GT/s (±10%) 2.5 GT/s (±10%)
Number of Lanes	
TLA7SA08	8 differential inputs, x4
TLA7SA16	16 differential inputs, x8
Record Length	TLA7SA16: 160M Symbols per differential input, 8 GB physical memory total (16 GB physical memory for a x16 configuration) TLA7SA08: 160M Symbols per differential input, 4 GB physical memory total 160M Symbols translates into 160 ms at 8 GT/s, 320 ms at 5 GT/s, or 640 ms at 2.5 GT/s at 100% bus utilization
Time Stamp Range	292 hours
Time Stamp	50 bits at 936 ps resolution
Clocking/Acquisition Modes	TLA module without SSC (Spread Spectrum Clocking), External Reference Clock (100 MHz ±10%) with or without SSC
External reference clock frequency tolerance	±300 ppm
Number of Mainframe Instrument Slots Required per TLA Series Module	2

Module Configuration Requirements

Module	Bi-directional Link Width			
	x1	x4	x8	x16
TLA7SA08	1	1	0	0
TLA7SA16	1	1	1	2

Input Characteristics (with P67SA00 Series Probes)

Characteristic	Description
Capacitive Loading	See P67SA00 Series Probe Manual
Minimum Data Eye	See P67SA00 Series Probe Manual

Acquisition Characteristics (with P67SA00 Series Probes)

Characteristic	Description
Dynamic Link-width Switch Latency	Consumes up to 48 symbols (typical)
Dynamic Link-rate Switch Latency	<200 ns EIDLE time (typical) (with either internal reference clock or spread spectrum using external reference clock) Maximum time to change to Gen1 rate: 2 TS1 Maximum time to change to Gen2 rate: 1 EIEOS + 3 TS1 Maximum time to change to Gen3 rate: 1 EIEOS + 6 TS1
Number of FTS Packets Required to Re-sync Following L0s Exit	Gen1*[1]: 4 FTS (typical) Gen2*[1]: 1 EIEOS + 6 FTS (typical) Gen3*[1]: 1 EIEOS + 4 FTS (typical)

*[1] Assumes an EIDLE ranging from 20 ns to 2 ms, with either internal reference clock or spread spectrum using external reference clock.

Filter Characteristics

Characteristic	Description
Ordered Sets	TS1, TS2, SKP, EIOS, FTS, EIEOS, SDS
DLLPs	Ack, Nak, PM, Vendor Specific, FC1, FC2, UpdateFC
TLPs	MRd, MRdL, MWr, IORd, IOWr, CfgRd0, CfgWr0, CfgRd1, CfgWr1, Msg, MsgD, Cpl, CplD, CPlLk, CPlDLk, FetchAdd, Swap, CAS, LPrfx, EPrfx

Trigger Characteristics

Characteristic	Description
Independent Trigger States	8
Trigger Sequencer Rate	Operates at symbol rate time (Gen1, Gen2, Gen3)
Maximum Independent If/Then Clauses per State	8
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Event Counters per State	2
Event Counter Range	31 bit
Number of TLP Packet Recognizers per Link Direction	4
Number of DLLP Packet Recognizers per Link Direction	4
Number of Sequence Recognizers	4
Number of Symbols per Sequence Recognizer	16
Number of Link Event Recognizers	4
Number of Global Counters/Timers	4
Trigger Event Types	Anything, TLP, DLLP, Sequence, Link Event, Counter, Timer
Trigger Action Types	Trigger, Trigger All Modules, Wait for System Trigger, Goto, Increment Counter, Decrement Counter, Reset Counter, Start Timer, Reset Timer, Reset and Start Timer, Stop Timer, Reset and Stop Timer, Set Signal Out, Clear Signal Out, Arm Module, Start Storage, Stop Storage, Do Nothing
Counter/Timer Range	48 bit (~5 days with 3.6 ns resolution)
Counter/Timer Test Latency	68 ns
Storage Control (Data qualification)	By state (start/stop)

Physical Characteristics

Dimensions	TLA7SA16		TLA7SA08	
	mm	in.	mm	in.
Height	262	10.3	262	10.3
Width	61	2.4	61	2.4
Depth	381	15	381	15
Weight	**kg**	**lb.**	**kg**	**lb.**
Net	3.20	7.06	2.84	6.25
Shipping	7.30	16.1	6.94	15.3

P67SA00 Series Probes

General

Characteristic	P67SA08	P67SA16	P67SA08G2	P67SA16G2	P67SA01S	P67SA04S	P67SA08S	P67SA16S	P67SA01SD	P67UHDSMA
Probe Type	PCI Express Midbus Differential Data	PCI Express Midbus Differential Data	PCI Express Midbus Differential Data	PCI Express Midbus Differential Data	PCI Express Slot Interposer	PCI Express Slot Interposer	PCI Express Slot Interposer	PCI Express Slot Interposer	PCI Express Differential Solder-down Probe	Probe lead set for PCI Express P67SA00 Series probe connections to high-bandwidth oscilloscopes
Number of Differential Pairs	8	16	8	16	2	8	16	32	1	4
Lane Width	x4	x8	x4	x8	x1	x4	x8	x16	1/2 lane	x2
Recommended Use	Recommended where signal integrity is critical	Recommended where signal integrity is critical	Recommended for midbus probing of PCIe Gen2	Recommended for midbus probing of PCIe Gen2	Recommended for platforms with no midbus footprints and the PCI Express slot is the only probe access point	Recommended for platforms with no midbus footprints and the PCI Express slot is the only probe access point	Recommended for platforms with no midbus footprints and the PCI Express slot is the only probe access point	Recommended for platforms with no midbus footprints and the PCI Express slot is the only probe access point	Recommended for platforms with no midbus footprint, PCI Express slot; or where space is limited	Recommended for use with any of the P67SA00 Series probe connections to high-bandwidth oscilloscopes
Attachment to Target System	Compression Technology	Compression Technology	—	—	PCI Express Slot	PCI Express Slot	PCI Express Slot	PCI Express Slot	Solder Down	—
Probe Loading AC/DC	See PCIe3 LPA Instruction Manual									—
Cable Length	1.8 m (6 ft.)									0.3 m (1 ft.)

Midbus Probe Recommended Configuration

x1	x4	x8	x16
1 P67SA08 1 TLA7SA08	1 P67SA08 1 TLA7SA08	1 P67SA16 1 TLA7SA16	2 P67SA16 2 TLA7SA16

Solder-down Probe Recommended Configurations

x1	x4	x8	x16
2 P67SA01SD 1 TLA7SA08	8 P67SA01SD 1 TLA7SA08	16 P67SA01SD 1 TLA7SA16	32 P67SA01SD 2 TLA7SA16

Slot Interposer Probe Recommended Configurations

x1	x4	x8	x16
1 P67SA01S 1 TLA7SA08	1 P67SA04S 1 TLA7SA08	1 P67SA08S 1 TLA7SA16	1 P67SA16S 2 TLA7SA16

Ordering Information

TLA7SA00 PCI Express Logic Protocol Analyzer Modules

Includes: Statement of Compliance, one-year warranty (return to Tektronix), reference clock cable (672-6285-xx), and reference clock jumper cable (174-5392-xx).
Probes, mainframes, and software must be ordered separately.

Module	Description
TLA7SA16	16 Differential Inputs, x8 Logic Protocol Analyzer module, 8 GT/s acquisition, 8 GB physical memory
TLA7SA08	8 Differential Inputs, x4 Logic Protocol Analyzer module, 8 GT/s acquisition, 4 GB physical memory

Note: Requires a TLA7012 or TLA7016 mainframe with TLA software v5.7 or above.

TLA7SA00 PCI Express Software

Software	Description
TMS160PCIE3	TLA protocol software for PCIe 3.0

Logic Analyzer TLA7SA00 Module Options

Option	Description
Opt. 88	Factory Install
Opt. L0	English manual
Opt. L5	Japanese manual
Opt. L10	Russian manual
Opt. L99	No manual

Service Options

The following service options are offered for the TLA logic analyzer products.

Option	TLA7SA00 Modules
Opt. CA1 provides a single calibration event or coverage for the designated calibration interval, whichever comes first	X
Opt. C3 Calibration Service 3 Years	X
Opt. C5 Calibration Service 5 Years	X
Opt. D1 Calibration Data Report	
Opt. D3 Calibration Data Report 3 Years (with Opt. C3)	
Opt. D5 Calibration Data Report 5 Years (with Opt. C5)	
Opt. R3 Repair Service 3 Years	X
Opt. R5 Repair Service 5 Years	X
Opt. S1 On-site Service 1 Year	
Opt. S3 On-site Service 3 Years (with R or C options)	
Opt. R1PW Repair Service Coverage 1-year Post Warranty	X
Opt. R2PW Repair Service Coverage 2-year Post Warranty	X
Opt. R3DW Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of instrument purchase	X
Opt. R5DW Repair Service Coverage 5 Years (includes product warranty period). 5-year period starts at time of instrument purchase	X

Recommended Accessories

Accessory	Description
P67SA08	8 Differential Pairs PCI Express Midbus Probe and Accessories **Includes**: Statement of Compliance, (2) 8-channel Retention Mechanisms, Velcro Cable Managers, Probe Instruction Manual
P67SA16	16 Differential Pairs PCI Express Midbus Probe and Accessories **Includes**: Statement of Compliance, (2) 16-channel Retention Mechanisms, Velcro Cable Managers, Probe Instruction Manual
P67SA08G2	8 Differential Pairs PCI Express Midbus Probe and Accessories for PCIe Gen2 **Includes**: Statement of Compliance, (2) 8-channel Retention Mechanisms, Velcro Cable Managers, Probe Instruction Manual
P67SA16G2	16 Differential Pairs PCI Express Midbus Probe and Accessories for PCIe Gen2 **Includes**: Statement of Compliance, (2) 16-channel Retention Mechanisms, Velcro Cable Managers, Probe Instruction Manual
P67SA01S	x1 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe Instruction Manual
P67SA04S	x4 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe Instruction Manual
P67SA08S	x8 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe Instruction Manual
P67SA16S	x16 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe Instruction Manual
P67SA01SD	Single Differential Input PCI Express Solder-down Probe **Includes**: Statement of Compliance, Velcro Cable Managers, Probe Instruction Manual Option 1P: Probe Power Adapter (1 required for every eight (8) P67SA01SD probes)
P67UHDSMA	x2 PCI Express Probe Lead Set for P67SA00 probe connections to oscilloscopes

P67SA00 Series Midbus Probes Standard Accessories

	P67SA08		P67SA16	
Description	Qty. per Probe	Part Number	Qty. per Probe	Part Number
Retention Mechanisms	1	020-4008-00	1	020-4016-00
Probe Adjustment Tool	1	003-1890-xx	1	003-1890-xx
Velcro Cable Manager (Bag of 2)	1	346-0300-xx	1	346-0300-xx

P67SA01SD Solder-down Standard Accessories

Description	Qty. per Probe	Part Number
TriMode™ Long Reach Solder Tip	1	P75TLRST
Storage Case	1	016-2009-xx
Solder Tip Tape (Strip of 10)	1	006-8237-xx
1 – .004 wire / 1 – .008 wire / 1 – SAC305 Solder (Package of 3 bobbins)	1	020-2754-xx
Hook and Loop fastening straps and dots	1	016-1953-xx
Installation Sheet	1	071-2503-xx

P67SA01SD Solder-down Required Accessories

Description	Qty.*2	Part Number
Power Adapter	1	870-0509-00

*2 See Solder-down Probe Configuration for Required Quantities.

P67SA01SD Solder-down Optional Accessories

Description	Qty.	Part Number
Bullet Removal Tool	1	003-1896-xx
Replacement Bullet Contacts	Pack of 4	003-0359-xx

CE

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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