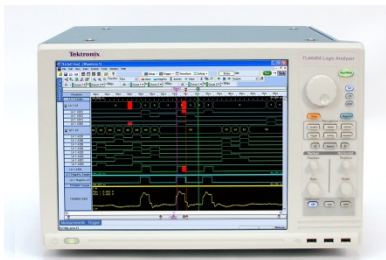


# TLA6400 Series Logic Analyzer Fact Sheet

The Perfect Blend of Performance, Ease of Use, and Affordability



## Features

## Benefits

### Performance and Ease of Use To Debug Today's Digital Systems

MagniVu™ acquisition

Accurately determine signal relationships with high sampling resolution (40 ps) on all channels

Automated measurements

Easily summarize your design's performance with sophisticated measurements such as: frequency, period, pulse width, duty cycle, and edge count

Drag & drop triggers

Quickly isolate events through simple and intuitive trigger setup. Triggers include: Channel Edge, Channel Value, Bus Value, Multi-Group Value, Glitch, Setup and Hold Violation, or Trigger on Anything

### Comprehensive Signal Integrity Debug Toolkit with:

Glitch Trigger, Capture and Display

Quickly find signal integrity problems by triggering on common problems such as crosstalk and termination errors. Exclusive glitch display removes need to manually search all channels by showing both the time and channel where any signal integrity problems occurred

iCapture™ multiplexing

Eliminate double probing and see both digital and analog acquisitions through a single logic analyzer probe

iView™ display

Gain complete system visibility with time-correlated, integrated analog and digital data on one display

## TLA6400 – A Significant Price-Performance Breakthrough



Featuring:

- iCapture™ eliminates messy double probing of signals
- iView™ time-correlated digital-analog view to clearly see how analog anomalies affect your digital signals
- Up to 667MHz state acquisition provides analysis of high-speed synchronous digital circuits
- 312.5 ps (3.2 GHz) with 64 Mb timing record length to capture intermittent events over a wide time window
- 40 ps-resolution MagniVu™ acquisition simultaneous with timing or state acquisition to find elusive timing problems quickly, without double probing
- Automated drag-and-drop measurements ensure faster setup and analysis for common tasks
- Drag-and-drop triggers simplify the task of isolating problems and data of interest

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## Key specifications and ordering information

Models	Channels (per module)	State Clock Rate	Record Length (Full CH)	Timing (Half/Full CH)	Timing (MagniVu™ acquisition)
TLA6401	34	333MHz (std) 667MHz (opt)	2Mb (std), 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	312.5ps / 625ps	40 ps
TLA6402	68	333MHz (std) 667MHz (opt)	2Mb (std), 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	312.5ps / 625ps	40 ps
TLA6403	102	333MHz (std) 667MHz (opt)	2Mb (std), 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	312.5ps / 625ps	40 ps
TLA6404	136	333MHz (std) 667MHz (opt)	2Mb (std), 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	312.5ps / 625ps	40 ps



Key Options	
Opt. 1S	Increase to 4 Mb base record length per channel
Opt. 2S	Increase to 8 Mb base record length per channel
Opt. 3S	Increase to 16 Mb base record length per channel
Opt. 4S	Increase to 32 Mb base record length per channel
Opt. 5S	Increase to 64 Mb base record length per channel
Opt. 1T	Increase to 667MHz State Speed
Opt. AM	Enable Full Analog Multiplexer
Opt. 18	Add Touchscreen
Opt. 1C	Add GPIB iView™ external oscilloscope interface kit
Opt. 2C	Add USB iView™ external oscilloscope interface kit
Opt. R3/R5	3 or 5 year repair service plan

Recommended Accessories	
PG3L	Digital pattern generator in a separate chassis
LACART	Accessory Cart
K4000	2 Shelf Accessory Cart
650-4815-xx	Additional Removable Hard Drive Assembly (No SW)
020-2664-xx	Rack Mount Kit



Spare Removable Hard Drive



Rack Mount Kit



LACART



K4000

### Key Applications

- FPGA
- Processor and Bus Debug and Verification
- Signal integrity

### Benefits

- Easily measure signals inside Altera or Xilinx FPGA designs and select which group of internal signals to probe without having to recompile
- View complete operation of today's complex designs: physical layer, timing, bus transactions and software execution.
- Find elusive glitches and events with MagniVu™ acquisition's high speed timing resolution of up to 40 ps