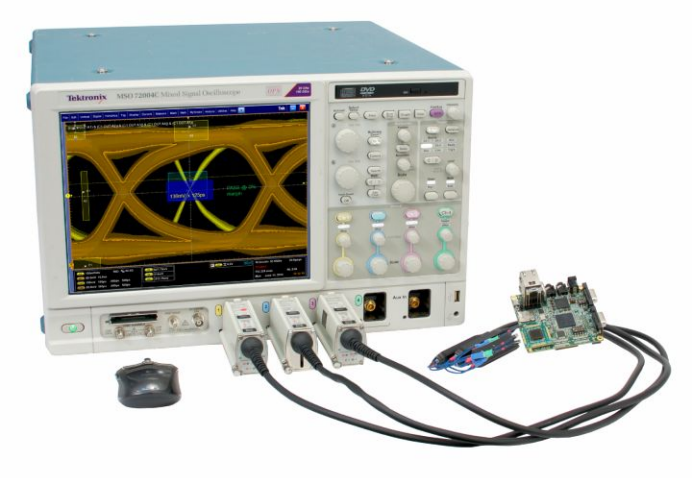
Memory Interface Electrical Verification and Debug

DDRA Datasheet



DDR Analysis is a standard specific solution tool for Tektronix Performance Digital Oscilloscopes (DPO7000C or DSA/DPO/MSO70000C/D/DX series). DDR Analysis requires Jitter and Eye Diagram Analysis Tool (Option DJA) and the advanced Search and Mark capability (Option ASM). The DDRA application includes compliance measurements and enables you to achieve new levels of productivity, efficiency, and measurement reliability.

Key features

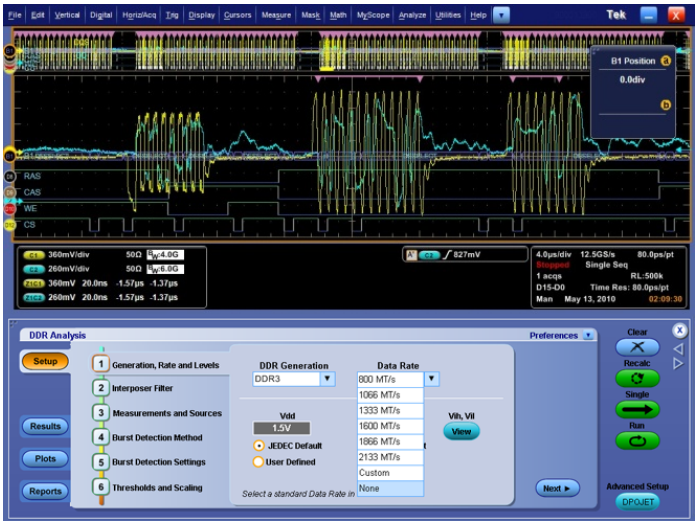
- Memory Validation and Debug: Comprehensive support for validation of multiple memory standards including DDR4 and LPDDR3
- Selectable Speed Grades: Support for JEDEC defined speed grades as well as custom speeds
- Auto Configuration Wizard: Easily set up the test configuration for performing electrical validation
- Qualified Multi-Rank Measurements: Measurements can be done on a selected rank of interest
- Visual Trigger Integration in DDRA: Quickly setup a Visual Trigger definition for an event of interest and use this definition to gate the measurements performed by DDRA
- Cycle Type Identification: Navigate and timestamp all acquired read and write cycles
- Read & Write Burst Trigger Events: Quickly and easily isolate DQ, DQS and Clock signals using graphical based trigger systems
- De-embedding: Quickly select and apply De-embedding filters from within DDRA to de-embed interposer and probe effects to accurately represent the signal
- Flexible Test Selection: Select the Memory specification and the Speed Grade for targeted analysis
- Reporting: Automatically generate comprehensive reports that include pass/fail results
- Verification and Debug: Quickly switch between verification debug mode for deeper root cause analysis using DPOJET
- Probing Solutions: A wide range of probing solutions including solder tips, BGA interposers and MSO interposers
- Address/Command Bus Capture: The digital channels on the MSO5000 or MSO70000 Series Mixed Signal Oscilloscope can be used to precisely qualify timing of different types of DDR bus cycles
- Programmable Interface: Allows development of remote client support for memory test

Applications

Validating the memory interface at the physical layer for signal integrity as well as timing to achieve the desired level of power / performance goals as well as for interoperability.

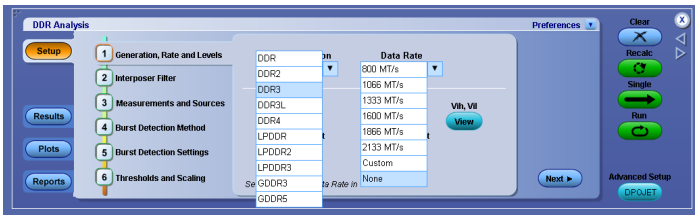
Option DDRA on the DSO/MSO5000, DPO7000 and DPO/MSO70000 series of Oscilloscopes provides support for multiple memory standards at JEDEC defined speed grades as well as custom speeds. The following Memory standards are supported by DDRA:

- DDR, DDR2, DDR3, DDR3L, DDR4
- LPDDR, LPDDR2, LPDDR3
- GDDR3, GDDR5



DDRA configuration wizard

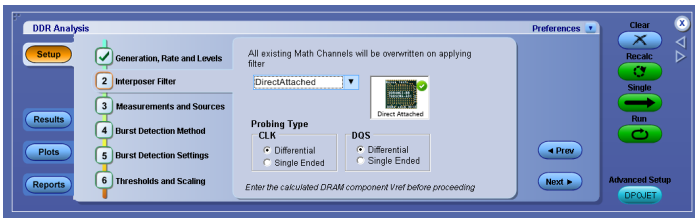
The configuration wizard in DDRA provides a simple, step-by step and easy to use interface to speed up the test process. The user selects the memory technology of interest, speed grade, measurement group (Reads, Writes, Clocks, Address and Control Lines) and individual measurements within the group from the DDRA user interface.



DDRA configuration

De-embed filters

Easily de-embed the Interposer and the Probe effects by applying suitable de-embed filters from within DDRA. DDRA also provides an option to apply custom filters.



De-embed filters

Comprehensive measurements

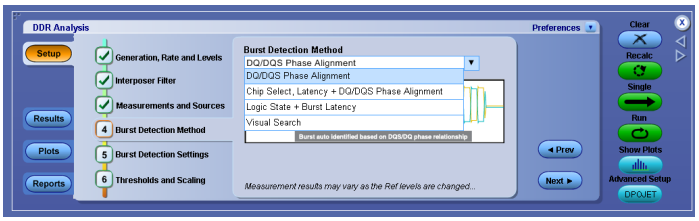
Option DDRA adds a long list of JEDEC specific measurements for different memory standards to the already existing rich tool set of generic jitter, timing and signal quality measurements in DPOJET.

Memory type	JEDEC specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79- 3F
DDR3L	JESD79-3-1
DDR4	JESD79-4A
LPDDR	JESD209B
LPDDR2	JESD209-2E
LPDDR3	JESD209-3B
GDDR5	JESD212

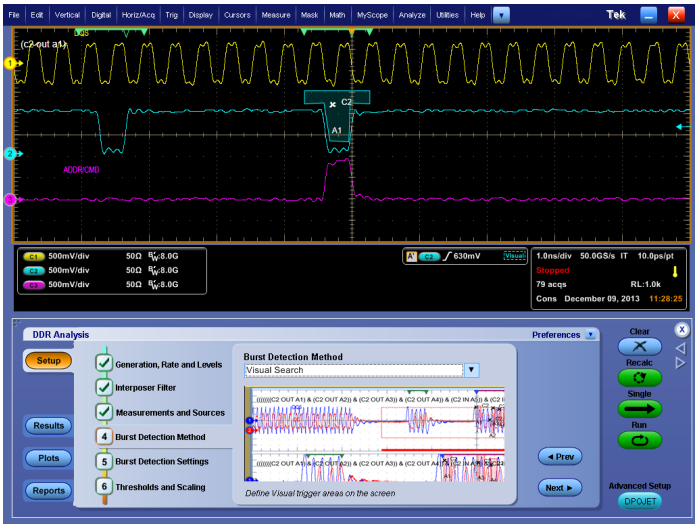
Burst detection

DDRA provides different ways to detect bus cycles that will be used to make measurements:

- Built-in algorithms identify Read/Write cycles based on the DQ/DQS phase difference
- Qualify this with Chip Select for analysis targeted at specific Ranks
- MSO digital channel based Command Identification for Read/Write detection
- Defining Visual Trigger Areas to identify and gate area of interest for measurement



Burst detection

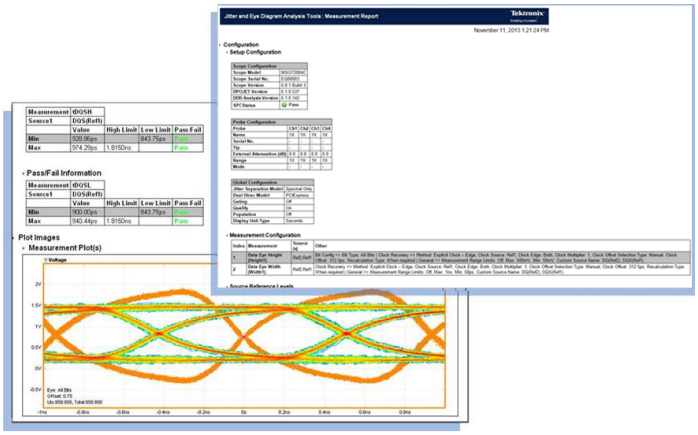


Visual trigger

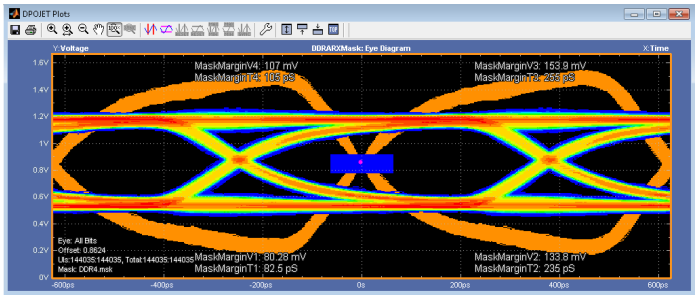
Results and reporting

Measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements based on the memory specification and the speed grade selected. The results are included in statistics and plots to provide a complete analysis of the acquired waveform.

Hyperlinks within the report allow easy navigation between different sections in order to co-relate different measurement results.



DDRA reports

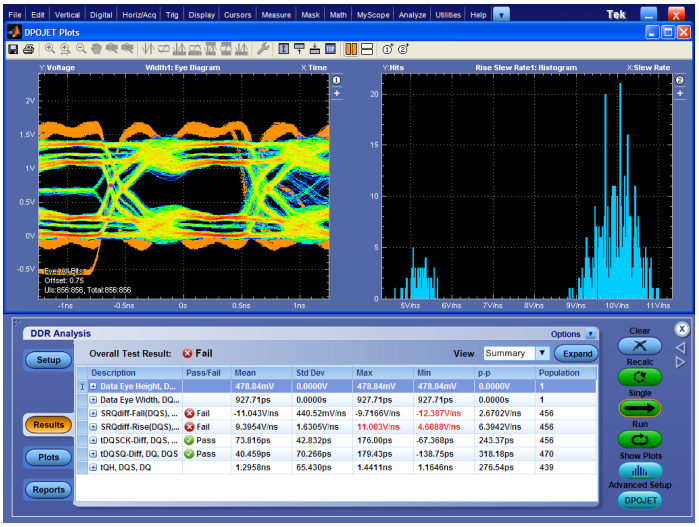


DDR4 mask margin

Verification versus debug

DDRA provides a comprehensive set of JEDEC measurements for different memory standards. In addition to this, it also provides access to the DPOJET advanced Jitter and Timing analysis engine that allows flexibility to reconfigure the existing measurements or to perform new measurements not defined by the JEDEC specification using new user specified test limits.

Also, features like logging, filters, histograms and time trends are available in DPOJET. This allows switching seamlessly between debug mode and verification mode.

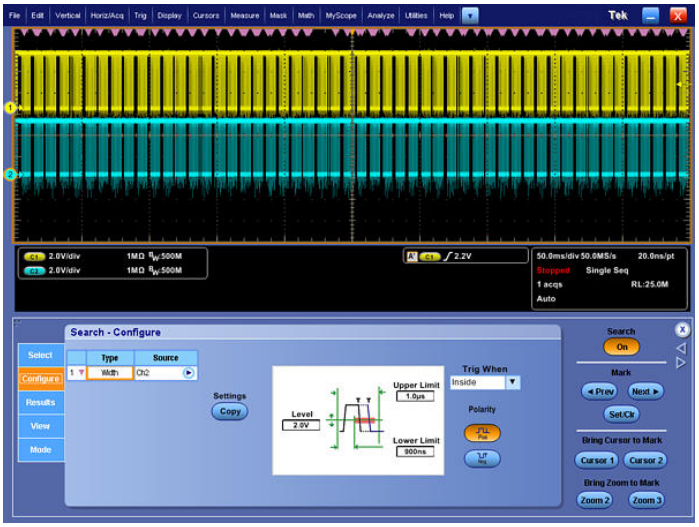


Memory interface analysis in DPOJET

Oscilloscope triggering and waveform identification

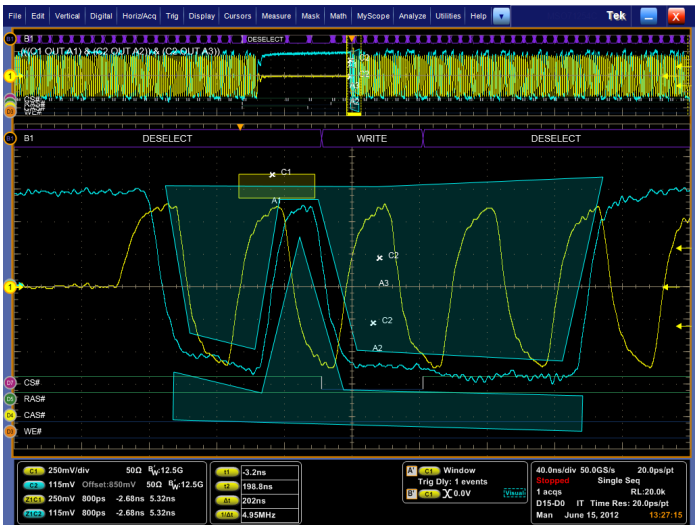
Tektronix Pinpoint® trigger system provides the most comprehensive high performance trigger system in the Industry. The Pinpoint trigger system encompasses threshold and timing related triggers, Dual A- and B-Event Triggering, Logic Qualification, Window Triggering, and Reset Triggering.

The Advanced Search and Mark feature on the Tektronix MSO/DPO5000, DPO7000, and MSO/DPO70000 Series Oscilloscopes finds unique events in waveforms. It scans acquired waveform data for multiple occurrences of an event and marks each occurrence. Search and Mark features have a close relationship with the Pinpoint trigger system since they both can be used to discriminate signal characteristics. Search and Mark includes signal-shape discrimination features of the Pinpoint trigger system and extends them across live channels, stored data and math waveforms.



Pinpoint triggering

Visual Trigger makes the identification of the desired waveform events quick and easy by scanning through all acquired analog waveforms and graphically comparing them to geometric shapes on the display. By discarding acquired waveforms which do not meet the graphical definition, Visual Triggering extends the oscilloscope's trigger capabilities beyond the traditional hardware trigger system.



Graphical triggering using Visual Trigger

These capabilities of the oscilloscope are very useful during the debug and are also extensively used by DDRA during the analysis.

Additional capabilities using a Performance Mixed-Signal Oscilloscope

The Mixed Signal Oscilloscope allows probing more signals on the memory bus and to trigger on and view specific bus events. With a Tektronix MSO5000 or MSO70000 Series Oscilloscope, up to 16 digital channels can be used to view logic states of command and address signals such as RAS, CAS, WE, CE, CS, etc.

On the MSO70000, signal integrity of these 16 inputs can be analyzed using the iCapture™ multiplexing feature, which allows any of the digital input signals to be internally routed to one of the scope's four analog channels. Measurements involving command-bus cycle timing can also be analyzed using the bus-decode features of the MSO and DDRA software.

MSO70000 Series Oscilloscope probing command signals

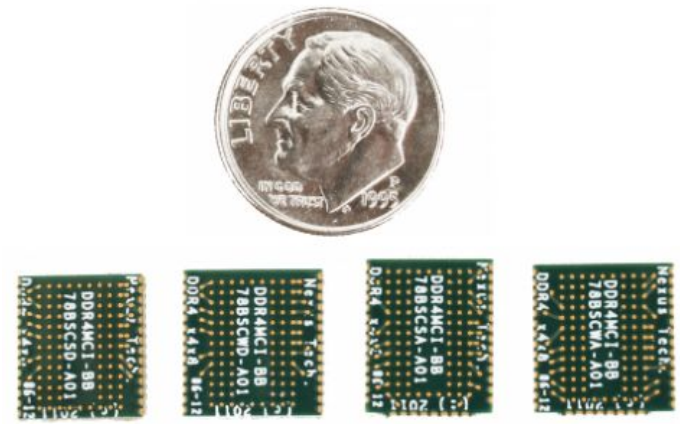
Probing

In order to perform analysis on the memory bus, access to the signal plays a very important role. JEDEC specification requires that the signals be probed at the balls of the memory device which are difficult to access.

To overcome this problem Tektronix, in partnership with Nexus Technology, is offering a variety of probing options such as BGA interposers that support different memory devices in a variety of form factors. The interposers include an embedded tip resister placed very close to the BGA pad.

Introduction of an interposer and the oscilloscope probe may change the characteristics of the signal. De-embedding filters can be used to remove the effect of the interposer and the probe in the signal path to get an accurate representation of the signal at the probe point.

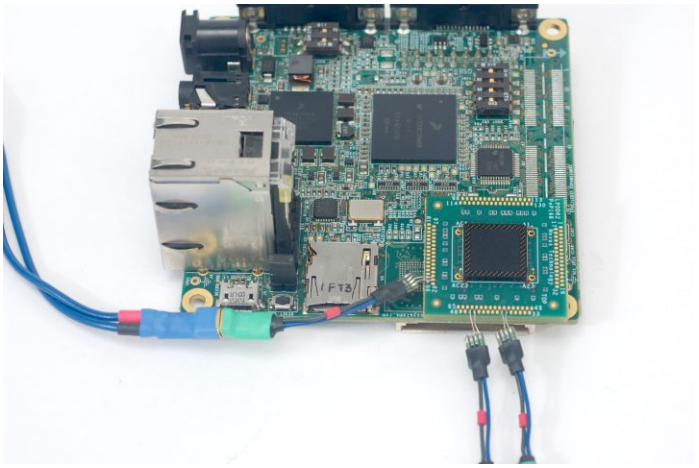
Technology	Package / form factor
DDR2	Socketed – 60 Ball / 84 Ball Solder-down – 60 Ball / 84 Ball
DDR3	Socketed – 78 Ball / 96 Ball Solder-down – 78 Ball / 96 Ball Edge Probe – 78 Ball / 96 Ball DIMM Interposer for MSO SO-DIMM Interposer for MSO
DDR4	Socketed – 78 Ball / 96 Ball Edge Probe – 78 Ball / 96 Ball Edge Probe – 144 Ball DIMM Interposer for MSO
LPDDR	Socketed – 60 Ball
LPDDR2	Socketed – 136 Ball / 168 Ball / 216 Ball / 240 Ball
LPDDR3	Socketed – 216 Ball Solder-down – 178 Ball
GDDR5	Socketed – 170 Ball Solder-down – 170 Ball



DDR4 Direct Attach Component Interposers (sizing relative to US coin)

P7500 Series Trimode™ Probe System with accessories

P7300 Series Z-Active™ Differential Probe System with accessories



LPDDR2 component package on package interposer

Logic debug and protocol analysis

When full protocol analysis or probing of the entire memory bus is required, a logic analyzer can provide this capability. The TLA7000 Series logic analyzers can also be linked with Tektronix oscilloscopes to provide an integrated test setup using tools such as iCapture mentioned above.

This eliminates the need for double probing and allows full analog capture of any signals probed by the logic analyzer. In addition, the iView™ display interface allows transfer of the oscilloscope data to the logic analyzer display, so that data from both instruments are analyzed and time-aligned on one display screen. Various types of probing solutions are available to support different form factors.

TLA Logic Analyzer and Probes for multichannel signal capture

Oscilloscope bandwidth considerations for memory analysis

(Category) specifications

Memory technology	DDR	DDR2	DDR2	DDR3	DDR3	DDR3L	LPDDR3	DDR4
Speed	all rates	to 400MT/s	to 800MT/s	to 1600MT/s	to 2400MT/s	to 1600MT/s	to 1600MT/s	to 3200MT/s
Max slew rate	5	5	5	10	12	12	8	18
Typical V swing	1.8	1.25	1.25	1	1	0.9	0.6	0.8
20-80 risetime (ps)	216	150	150	60	50	45	45	27
Equivalent Edge BW	1.9	2.7	2.7	6.7	8.0	8.9	8.9	15.0
Recommended Scope BW (max performance) [1]	2.5	3.5	4.0	12.5	12.5	12.5	12.5	16
Recommended scope BW (typical performance) [2]	2.5	2.5	3.5	8.0	12.5	12.5	12.5	12.5

1 Highest accuracy on faster slew rates.

2 Slew rates are about 80% of the max specification. DDR3L, DDR4 and LPDDR3 is supported only on MSO/DPO70000C/D models only.

Ordering information

Models

DDRA	DDR Memory Bus Electrical Validation and Analysis Oscilloscope Software.

To order on a new DPO/MSO5000, DPO7000, DPO/MSO70000 Series:

Option DDRA	Preinstall on a new DPO5000 [3], MSO5000 [3], DPO7000 [3], DPO70000 [3], or MSO70000 [3] Series oscilloscope
DPOFL-DDRA	DDR Memory Technology Analysis Package – Floating License

To order on existing DPO/MSO5000, DPO7000, DPO/MSO70000 Series:

DPO-UP DDRA	Upgrade to Option DDRA (requires Options ASM and DJA)
DPO-UP DJAE	Upgrade MSO/DPO5000 Series with DPOJET Jitter and Eye Diagram Analysis (Option DJA)
DPO-UP DJAM	Upgrade DPO7000 with DPOJET Jitter and Eye Diagram Analysis (Option DJA)
DPO-UP DJAH	Upgrade DPO70404 - DPO70804 or MSO70404 - MSO70804 with DPOJET Jitter and Eye Diagram Analysis (Option DJA)
DPO-UP DJAU	Upgrade DPO71254 - DPO73304 or MSO71254 - MSO72004 with DPOJET Jitter and Eye Diagram Analysis (Option DJA)
DPO-UP DJUP	DJA DPOJET software for oscilloscopes with both TDSJIT3 and TDSRTE licenses

To order floating licenses on existing DPO/MSO5000, DPO7000, DPO/MSO70000 Series:

DPOFL-DDRA	DDRA Package – Floating License
DPOFL-DJA	DPOJET Jitter and Eye Diagram Analysis – Floating License

Recommended accessories

P7500 Series	TriMode™ Differential Probe
020-2955-xx	Micro-coax Tips (TriMode) for P7500 Series Probes
020-3022-xx	Micro-coax Tips (TriMode) for P7500 Series Probes [4]
020-2954-xx	Socket Cable for P7500 Series Probes
P7300 Series	Z-Active™ Differential Probe (P7313, P7340A, P7360A, or P7380A)
020-2600-xx	Short Flex, Small Resistor Tip-Clip Assembly for P7300 Series Probes
020-2602-xx	Medium Flex, Small Resistor Tip-Clip Assembly for P7300 Series Probes
020-2604-xx	Long Flex, Small Resistor Tip-Clip Assembly for P7300 Series Probes
006-3415-xx	Antistatic Wrist Strap for P7300 Series Probes
P6780	Differential Logic Probe for MSO70000 Series Oscilloscopes
TDP3500	Differential Probe for MSO/DPO5000 and DPO7000 Series Oscilloscopes

3 DDR3L, DDR4 and LPDDR3 are supported only on MSO/DPO70000C/D models.

4 For use with BGA Interposers only.

BGA interposers – by memory standard

DDR2	x4, x8, x16 socketed and solder down interposers
DDR3	x4, x8,16 socketed, solder down and direct attach interposers
DDR4	x4, x8,16 socketed, solder down and direct attach interposers
LPDDR2	BGA and PoP Interposers
LPDDR3	BGA and PoP Interposers
GDDR5	Solder Down and Socketed Interposers

CE

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