# Die Attach Equipment and ESD

***Our thanks to SIMCO for allowing us to reprint the following article.***

**OVERVIEW:**

In semiconductor manufacturing, the die attach operation takes the singulated chips from the wafer and places them in a new target location (such as a tray, substrate, printed circuit board, etc.). Four general categories of ESD failure modes have been observed at this operation, namely: Charged Device Model (CDM), Field Induced Model (FIM), Machine Model (MM), and Charged Board Model (CBM). We have identified seven distinct mechanisms in typical die attach operations that can and do cause ESD damage to the chips being handled. They are reviewed here.

First, to hold semiconductor wafers in place and to facilitate subsequent operations at wafer sawing, back grinding, scribing and breaking, wafer probing, die attach, and various pick and place operations, typical semiconductor procedures include the mounting of wafers on a sheet of adhesive tape material (blue tape is common) that is held in place by an outer metal ring assembly. As the adhesive tapes are insulative, they become highly charged whenever contact is made with the material. Charges of 20Kv and higher are typical from even just slight contact and separation (rubbing). This charging of the adhesive tape material, in turn, causes the wafer to become charged inductively. The devices on the wafer can be subsequently damaged when discharged by any large conductor such as operators, metal fixtures, robot arms, stages and chucks, etc.

The die-attach/chip-picking operations where the diced, individual chips are removed from the adhesive tape assemblies have been especially interesting from a device failure viewpoint. We have found this particular operation has resulted in perhaps more documented CDM ESD damage than any other single operation in typical semiconductor manufacturing processes. That statement is based on literally scores of case studies where this operation was analyzed…leading to documented yield improvements. And there is more to understanding the associated failure modes here than meets the eye. It has been determined that at least 7 different failure mechanisms to chips can exist here as we will describe in detail.

**1. Charging of Tape from Operator Handling:**

Operators or other types of handling mechanisms cause the adhesive tape material to become charged. The devices on the tape now diced from the wafer charge inductively and then become discharged either by operators (with tweezers typically) or the conductive collet on the automatic chip-picking equipment…causing CDM damage to the device.

**2. Recharging of Tape from Chip Picking:** Even if the charge on the tape is removed before the operation begins, another chip charging mechanism subsequently occurs. As each chip is lifted off the tape a resulting charge remains on the tape in that “missing chip” area.

As the chip removal operation advances, this “missing chip” area (exposed tape) increases and the field strength becomes more dangerous. The remaining chips become charged by induction from this field – and can be subsequently discharged. Typically the discharge occurs through the conductive collet on the equipment. In our past case studies the chips damaged from this mechanism tend to be located near the end of the picking process – as might be expected since the field strength becomes stronger and stronger as more and more chips are removed! Even if charge is removed on the tape assembly before the operation begins the tape will recharge during the chip picking process.

**3. Charging of Chips During Separation from Tape:**

An ionizer is typically employed to remove the charging mechanisms detailed in 1 and 2 above. A third charging mechanism exists during this operation…one that cannot be eliminated strictly by employing an ionizer above the chip picking collet. The next failure mode to be described has resulted in

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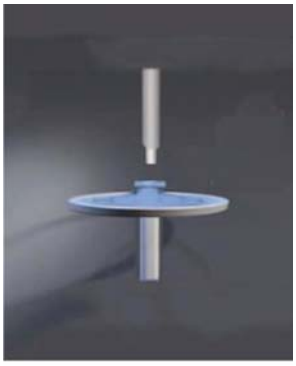
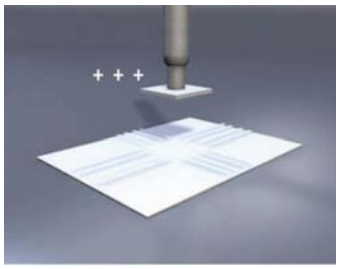
many cases of device damage – and it is not very well understood or addressed typically. (It is emphasized here that many process engineers now implement ionizers above the chip-picking collet so that ESD risks from the high charge generating nature of these tape assemblies are eliminated. However, the overhead ionizer cannot – and does not - eliminate this next risk!) As the chip is lifted off the tape, friction and separation can cause the chip to charge dramatically. We have measured (via Faraday cup measurements) chip charging in excess of 10 Kv from this event. This chip charging is especially dangerous as the conductive collet is already in contact with the chip and can cause an immediate discharge. This failure mode occurs so rapidly (nSec to uSec range) that standard ionizing techniques typically are not able to prevent the damage. We have been successful using the approach of changing the collet material to a less conductive material and implementing custom ionization. The custom ionization should be implemented so that the chip is discharged on its way from the separation point to its next conductive contact which is most likely a conductive container, a printed circuit board assembly, a substrate, etc., that can potentially discharge it. That distance can be short, and the operation can be rapid – so intelligent, custom, selection of the ionization device is essential in this case.

**4. Pogo Pin Discharge:**



Some die attach/chip-picking machines also include an additional “pogo pin” mechanism (that can be conductive) underneath the tape assembly. It is designed to push up the chip slightly so that the overhead collet has an easier time lifting the chip off the sticky tape surface. We have also verified chip damage that was traced to the discharging of the charged chip via this “pogo pin” although this failure mode has been observed less in our case studies. The signature damage “earmark” on these failures (SEM images, etc.) is dramatically different than the signature damage typical in failure mode #3 above, as might be expected from a top versus bottom discharge. It is important to note that there have been documented cases where discharges still occurred to the “pogo pin” with wafers/chips that had insulative bottom layers.

**5. Picked Chip Discharging Into Target Location:**



Once a chip has been “picked” (lifted off of the tape surface by the collet) on this type of equipment, it subsequently is transported via the moving collet to a target location on the machine such as a printed circuit board assembly, or a substrate, or a conductive container, tray, or waffle pack, etc. If the chip is still charged from any one of the mechanisms reviewed above, it can be damaged by a discharge at its target location. It is very important to insure that no charge remains on the chip before it is placed into its final resting place on the machine.

**6. Charged Target Location:** Yet another failure mode can exist with this type of equipment. Even if all of CDM risks addressed in modes 1-5 above are addressed and eliminated a Machine Model (MM) risk can be present if the target location has become charged. We have observed cases for example, where the chips were placed onto charged bare printed circuit boards (PCB’s). The PCB’s were initially charged from the processing operations leading up to their contact with the chip. Printed circuit wiring can discharge into the chip in this case…which is a “mini” machine model (MM) failure mode.

**7. Chips Recharging in Target Locations:** And finally, it is possible for the chips to become recharged and subsequently discharged before the final assembly leaves the die attach machine. The two most common causes of chip charging at this late stage are typically the result of existing charge on the printed circuit board plastic that inductively couples into the chips on the board and triboelectric charging of the entire assembly from sliding on a conveyer belt or other surface (CBM failure mode). It is important to verify that none of the above failure modes exist in this operation. We have verified (confirmed) yield losses on occasion from each of these seven failure modes.

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**SUMMARY:**

Substantial amounts of charged device model ESD damage are not only possible but are probable in semiconductor die attach operations if the necessary ESD controls are not in place. Yield losses due to CDM and MM electrical damage due to these operations can be substantial1. Eliminating the potential risks is critical for state-of-the-art reliability and profitable operations.

**REFERENCES:**

1. R.J.Peirce, “CDM ESD Failure Analysis,” *Solid State Technology*, May 2007.

**About the Author**

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